

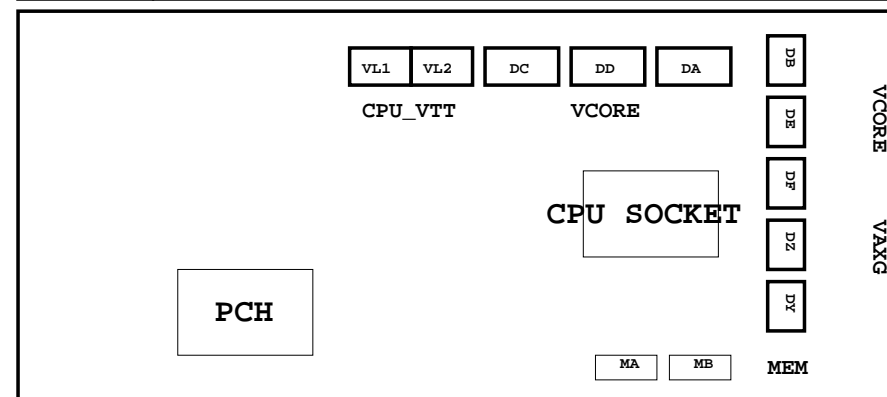
Model Name: GA-Z77X-UP4 TH 1.01

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE
10	PCH_DP_HDMI_DVI_DAC,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*1 SLOTS X3
18	PCI EXPRESS*16/*8/*4 SWITCH
19	IT8892 PCIE to PCI BRIDGE
20	PCI SLOT
21	HDMI / DVI Connector
22	mSATA Connector
23	Dual BIOS , TPM
24	Realtek 892
25	REAR AUDIO JACK
26	VCORE PWM_IR3567A -1
27	VCORE PWM_IR3567A -2

SHEET TITLE

28	DDR_15V & CPUVTT PWM_IR3570-1
29	DDR_15V & CPUVTT PWM_IR3570-2
30	DISCRETE POWER 1
31	DISCRETE POWER 2
32	I/O IT8728F
33	USB3 , KB/USB3, -PHOT
34	F_PANEL , F_USB , F_USB3
35	ATX POWER, CLOCK BUFFER
36	HWM, FAN CTRL
37	REALTEK 8111F
38	PLX PEX8605 PCIE*1 X3
39	OV NCT3933 / COM
40	VIA VL800
41	DP SWITCH
42	CACTUS RIDGE(THUNDERBOLT)
43	mDP -1
44	mDP -2
45	TABLE LIST

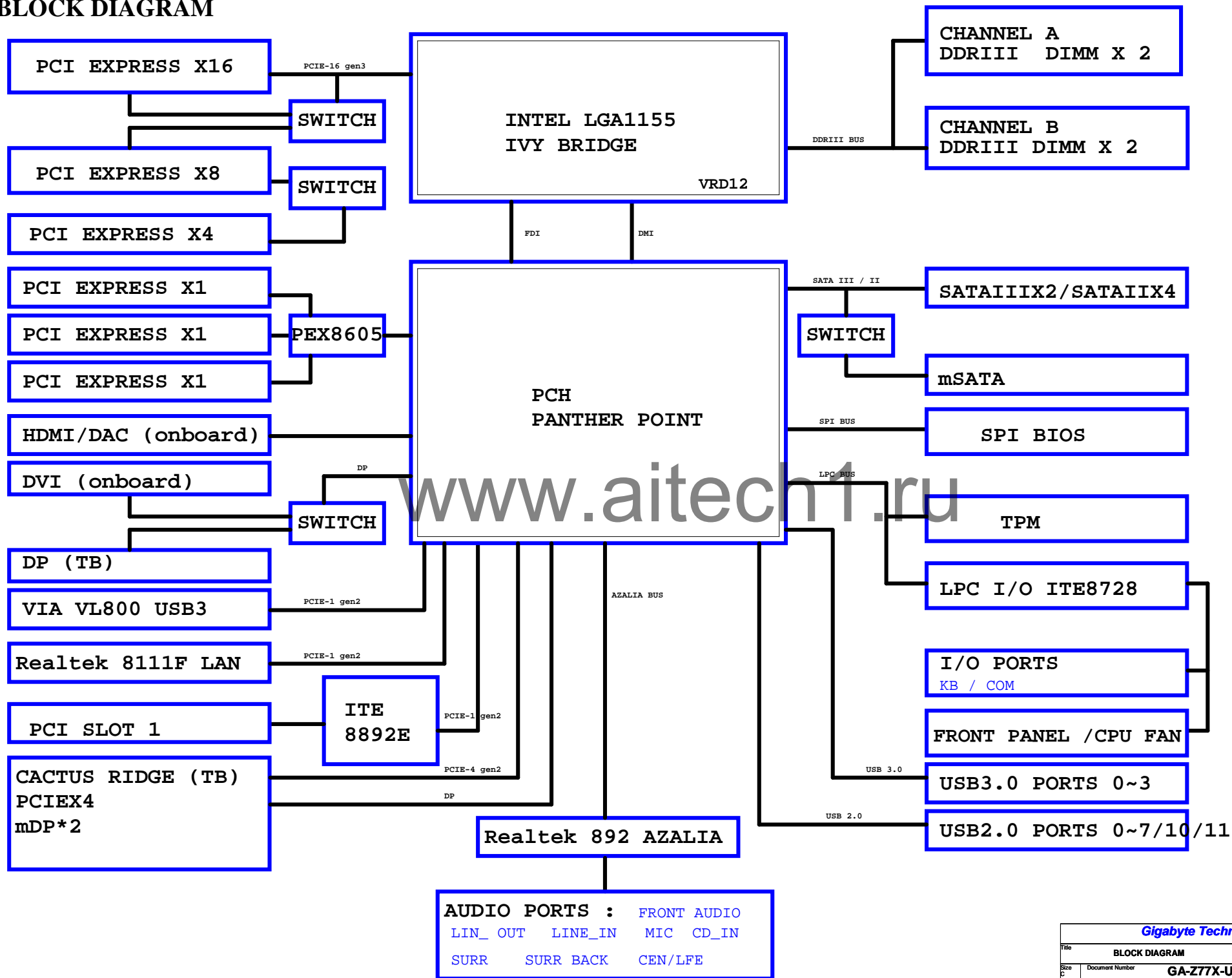


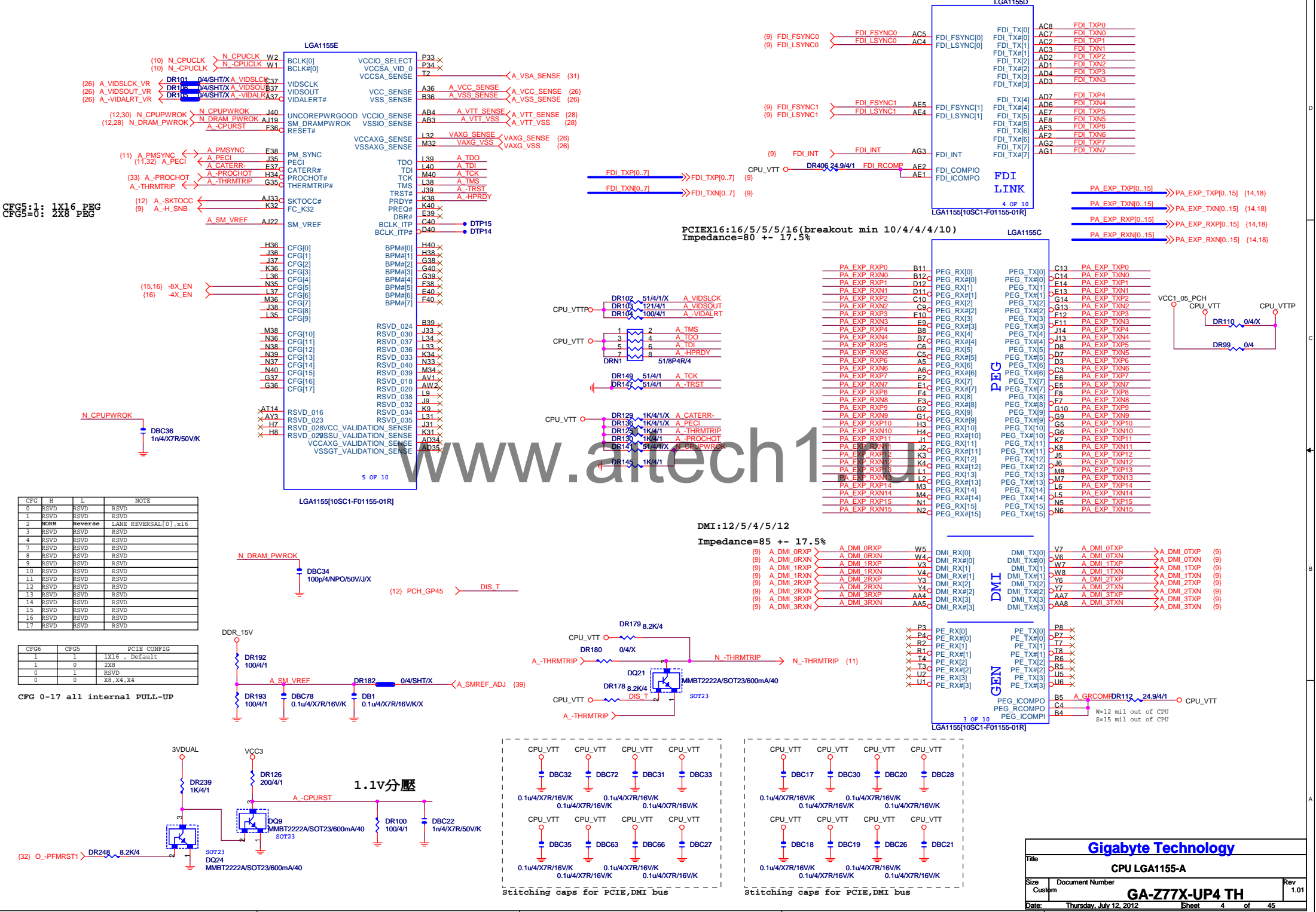
Component value change history

[illegible]

DATE	Change Item	Reason
2012/03/07	0.1 SCH modify from Z77X-UD3H VCOORE change PWRSTAGE 3550 11*11 choke + 820uF VTT change 1+1 / 2 phase TB 4C PLX8605 PCIE*1 SW Remove 9172 SATA3 PCIEX16/X8/X4 sharing COM port	Spec Change
2012/03/30	0.2 SCH modify LAN solution change to 8111F Codec soluion change to 892 VAXG Phase2 ISEN/RSEN link SWAP DP/DVI SW SCH modify	
2012/04/06	Add SPDIF_IN	
2012/04/17	CBC1/2/7/9 CHANGE 0603	
2012/07/12	PLX PCB footprint issue improve	

BLOCK DIAGRAM





CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	RSVD	Reverse	LANE REVERSAL[0], x16
3	RSVD	RSVD	RSVD
4	RSVD	RSVD	RSVD
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1x16, Default
1	0	2x8
0	1	RSVD
0	0	8x, 4x, 4x

CFG 0-17 all internal PULL-UP

LGA1155A

M_AAA0	AV27	SA_MA[0]	SA_DSQ[0]	AK3	M_DQSA0
M_AAA1	AY24	SA_MA[1]	SA_DSQ[0]	AK2	M_DQSA0
M_AAA2	AW24	SA_MA[2]			
M_AAA3	AW23	SA_MA[3]			
M_AAA4	AV23	SA_MA[4]	SA_DQ[1]	AJ3	M_DA0
M_AAA5	AT24	SA_MA[5]	SA_DQ[1]	AJ4	M_DA1
M_AAA6	AT23	SA_MA[6]	SA_DQ[2]	AJ3	M_DA2
M_AAA7	AU22	SA_MA[7]	SA_DQ[3]	AL4	M_DA3
M_AAA8	AV22	SA_MA[8]	SA_DQ[4]	AJ2	M_DA4
M_AAA9	AT22	SA_MA[9]	SA_DQ[5]	AJ1	M_DA5
M_AAA10	AV28	SA_MA[10]	SA_DQ[6]	AL2	M_DA6
M_AAA11	AU21	SA_MA[11]	SA_DQ[7]	AL1	M_DA7
M_AAA12	AT21	SA_MA[12]			
M_AAA13	AW32	SA_MA[13]	SA_DSQ[1]	AP3	M_DQSA1
M_AAA14	AU20	SA_MA[14]	SA_DSQ[1]	AP2	M_DQSA1
M_AAA15	AT20	SA_MA[15]			

(7)	M_SWEA	M_SWEA	AW29	SA_WE#
(7)	M_SCASA	M_SCASA	AV30	SA_CAS#
(7)	M_SRASA	M_SRASA	AU28	SA_RAS#

(7)	M_SBA0	M_SBA0	AY29	SA_BS[0]
(7)	M_SBA1	M_SBA1	AW28	SA_BS[1]
(7)	M_SBA2	M_SBA2	AV20	SA_BS[2]

(7)	M-CSA0	M-CSA0	AU29	SA_CS#0
(7)	M-CSA1	M-CSA1	AV32	SA_CS#1
(7)	M-CSA2	M-CSA2	AW30	SA_CS#2
(7)	M-CSA3	M-CSA3	AU33	SA_CS#3

(7)	M_CKEA0	M_CKEA0	AV19	SA_CKE[0]
(7)	M_CKEA1	M_CKEA1	AT19	SA_CKE[1]
(7)	M_CKEA2	M_CKEA2	AU18	SA_CKE[2]
(7)	M_CKEA3	M_CKEA3	AV18	SA_CKE[3]

(7)	M_ODT_A0	AV31	SA_ODT[0]
(7)	M_ODT_A1	AU32	SA_ODT[1]
(7)	M_ODT_A2	AU30	SA_ODT[2]
(7)	M_ODT_A3	AW33	SA_ODT[3]

(7)	M_DCLKA0	M_DCLKA0	AY25	SA_CK[0]
(7)	M_DCLKA1	M_DCLKA1	AW25	SA_CK[0]
(7)	M_DCLKA2	M_DCLKA2	AU24	SA_CK[1]
(7)	M_DCLKA3	M_DCLKA3	AW27	SA_CK[2]
(7)	M_DCLKA4	M_DCLKA4	AY27	SA_CK[3]
(7)	M_DCLKA5	M_DCLKA5	AV26	SA_CK[3]
(7)	M_DCLKA6	M_DCLKA6	AW26	SA_CK[3]

(7)	M_DCLKA7	M_DCLKA7	AW26	SA_CK[3]
(7)	M_DCLKA8	M_DCLKA8	AW26	SA_CK[3]
(7)	M_DCLKA9	M_DCLKA9	AW26	SA_CK[3]

(7)	M_DCLKA10	M_DCLKA10	AW26	SA_CK[3]
(7)	M_DCLKA11	M_DCLKA11	AW26	SA_CK[3]
(7)	M_DCLKA12	M_DCLKA12	AW26	SA_CK[3]

(7)	M_DCLKA13	M_DCLKA13	AW26	SA_CK[3]
(7)	M_DCLKA14	M_DCLKA14	AW26	SA_CK[3]
(7)	M_DCLKA15	M_DCLKA15	AW26	SA_CK[3]

(7)	M_DCLKA16	M_DCLKA16	AW26	SA_CK[3]
(7)	M_DCLKA17	M_DCLKA17	AW26	SA_CK[3]
(7)	M_DCLKA18	M_DCLKA18	AW26	SA_CK[3]

(7)	M_DCLKA19	M_DCLKA19	AW26	SA_CK[3]
(7)	M_DCLKA20	M_DCLKA20	AW26	SA_CK[3]
(7)	M_DCLKA21	M_DCLKA21	AW26	SA_CK[3]

(7)	M_DCLKA22	M_DCLKA22	AW26	SA_CK[3]
(7)	M_DCLKA23	M_DCLKA23	AW26	SA_CK[3]
(7)	M_DCLKA24	M_DCLKA24	AW26	SA_CK[3]

(7)	M_DCLKA25	M_DCLKA25	AW26	SA_CK[3]
(7)	M_DCLKA26	M_DCLKA26	AW26	SA_CK[3]
(7)	M_DCLKA27	M_DCLKA27	AW26	SA_CK[3]

(7)	M_DCLKA28	M_DCLKA28	AW26	SA_CK[3]
(7)	M_DCLKA29	M_DCLKA29	AW26	SA_CK[3]
(7)	M_DCLKA30	M_DCLKA30	AW26	SA_CK[3]

(7)	M_DCLKA31	M_DCLKA31	AW26	SA_CK[3]
(7)	M_DCLKA32	M_DCLKA32	AW26	SA_CK[3]
(7)	M_DCLKA33	M_DCLKA33	AW26	SA_CK[3]

(7)	M_DCLKA34	M_DCLKA34	AW26	SA_CK[3]
(7)	M_DCLKA35	M_DCLKA35	AW26	SA_CK[3]
(7)	M_DCLKA36	M_DCLKA36	AW26	SA_CK[3]

(7)	M_DCLKA37	M_DCLKA37	AW26	SA_CK[3]
(7)	M_DCLKA38	M_DCLKA38	AW26	SA_CK[3]
(7)	M_DCLKA39	M_DCLKA39	AW26	SA_CK[3]

(7)	M_DCLKA40	M_DCLKA40	AW26	SA_CK[3]
(7)	M_DCLKA41	M_DCLKA41	AW26	SA_CK[3]
(7)	M_DCLKA42	M_DCLKA42	AW26	SA_CK[3]

(7)	M_DCLKA43	M_DCLKA43	AW26	SA_CK[3]
(7)	M_DCLKA44	M_DCLKA44	AW26	SA_CK[3]
(7)	M_DCLKA45	M_DCLKA45	AW26	SA_CK[3]

(7)	M_DCLKA46	M_DCLKA46	AW26	SA_CK[3]
(7)	M_DCLKA47	M_DCLKA47	AW26	SA_CK[3]
(7)	M_DCLKA48	M_DCLKA48	AW26	SA_CK[3]

(7)	M_DCLKA49	M_DCLKA49	AW26	SA_CK[3]
(7)	M_DCLKA50	M_DCLKA50	AW26	SA_CK[3]
(7)	M_DCLKA51	M_DCLKA51	AW26	SA_CK[3]

(7)	M_DCLKA52	M_DCLKA52	AW26	SA_CK[3]
(7)	M_DCLKA53	M_DCLKA53	AW26	SA_CK[3]
(7)	M_DCLKA54	M_DCLKA54	AW26	SA_CK[3]

(7)	M_DCLKA55	M_DCLKA55	AW26	SA_CK[3]
(7)	M_DCLKA56	M_DCLKA56	AW26	SA_CK[3]
(7)	M_DCLKA57	M_DCLKA57	AW26	SA_CK[3]

(7)	M_DCLKA58	M_DCLKA58	AW26	SA_CK[3]
(7)	M_DCLKA59	M_DCLKA59	AW26	SA_CK[3]
(7)	M_DCLKA60	M_DCLKA60	AW26	SA_CK[3]

(7)	M_DCLKA61	M_DCLKA61	AW26	SA_CK[3]
(7)	M_DCLKA62	M_DCLKA62	AW26	SA_CK[3]
(7)	M_DCLKA63	M_DCLKA63	AW26	SA_CK[3]

DDR_0

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LGA1155[10SC1-F01155-01R]

LGA1155B

M_AAB0	AK24	SB_MA[0]	AH7	M_DQSB0
M_AAB1	AM20	SB_MA[1]	AH6	M_DQSB0
M_AAB2	AM19	SB_MA[2]		
M_AAB3	AK18	SB_MA[3]	AG7	M_DB0
M_AAB4	AP19	SB_MA[4]	AG8	M_DB1
M_AAB5	AP18	SB_MA[5]	AJ9	M_DB2
M_AAB6	AM18	SB_MA[6]	AJ8	M_DB3
M_AAB7	AL18	SB_MA[7]	AG5	M_DB4
M_AAB8	AL18	SB_MA[8]	AG6	M_DB5
M_AAB9	AY17	SB_MA[9]	AJ6	M_DB6
M_AAB10	AN23	SB_MA[10]	AJ7	M_DB7
M_AAB11	AU17	SB_MA[11]		
M_AAB12	AT18	SB_MA[12]	AM8	M_DQSB1
M_AAB13	AR26	SB_MA[13]	AL8	M_DQSB1
M_AAB14	AV16	SB_MA[14]		
M_AAB15	AV16	SB_MA[15]		

(8)	M_SWEB	M_SWEB	AR25	SB_WE#
(8)	M_SCASB	M_SCASB	AK25	SB_CAS#
(8)	M_SRASB	M_SRASB	AP24	SB_RAS#

(8)	M_SBA0	M_SBA0	AP23	SB_BS[0]
(8)	M_SBA1	M_SBA1	AM24	SB_BS[1]
(8)	M_SBA2	M_SBA2	AW17	SB_BS[2]

(8)	M-CSB0	M-CSB0	AN25	SB_CS#0
(8)	M-CSB1	M-CSB1	AN26	SB_CS#1
(8)	M-CSB2	M-CSB2	AL26	SB_CS#2
(8)	M-CSB3	M-CSB3	AT26	SB_CS#3

(8)	M_CKEB0	M_CKEB0	AU16	SB_CKE[0]
(8)	M_CKEB1	M_CKEB1	AY16	SB_CKE[1]
(8)	M_CKEB2	M_CKEB2	AW15	SB_CKE[2]
(8)	M_CKEB3	M_CKEB3	AV15	SB_CKE[3]

(8)	M_ODT_B0	AL26	SB_ODT[0]
(8)	M_ODT_B1	AP26	SB_ODT[1]
(8)	M_ODT_B2	AM26	SB_ODT[2]
(8)	M_ODT_B3	AK26	SB_ODT[3]

(8)	M_DCLKB0	M_DCLKB0	AL21	SB_CK[0]
(8)	M_DCLKB1	M_DCLKB1	AL22	SB_CK[0]
(8)	M_DCLKB2	M_DCLKB2	AL20	SB_CK[1]
(8)	M_DCLKB3	M_DCLKB3	AK20	SB_CK[2]
(8)	M_DCLKB4	M_DCLKB4	AL23	SB_CK[3]
(8)	M_DCLKB5	M_DCLKB5	AM22	SB_CK[3]
(8)	M_DCLKB6	M_DCLKB6	AP21	SB_CK[3]
(8)	M_DCLKB7	M_DCLKB7	AN21	SB_CK[3]

(8)	M_DCLKB8	M_DCLKB8	AL21	SB_CK[3]
(8)	M_DCLKB9	M_DCLKB9	AL21	SB_CK[3]
(8)	M_DCLKB10	M_DCLKB10	AL21	SB_CK[3]

(8)	M_DCLKB11	M_DCLKB11	AL21	SB_CK[3]
(8)	M_DCLKB12	M_DCLKB12	AL21	SB_CK[3]
(8)	M_DCLKB13	M_DCLKB13	AL21	SB_CK[3]

(8)	M_DCLKB14	M_DCLKB14	AL21	SB_CK[3]
(8)	M_DCLKB15	M_DCLKB15	AL21	SB_CK[3]
(8)	M_DCLKB16	M_DCLKB16	AL21	SB_CK[3]

(8)	M_DCLKB17	M_DCLKB17	AL21	SB_CK[3]
(8)	M_DCLKB18	M_DCLKB18	AL21	SB_CK[3]
(8)	M_DCLKB19	M_DCLKB19	AL21	SB_CK[3]

(8)	M_DCLKB20	M_DCLKB20	AL21	SB_CK[3]
(8)	M_DCLKB21	M_DCLKB21	AL21	SB_CK[3]
(8)	M_DCLKB22	M_DCLKB22	AL21	SB_CK[3]

(8)	M_DCLKB23	M_DCLKB23	AL21	SB_CK[3]
(8)	M_DCLKB24	M_DCLKB24	AL21	SB_CK[3]
(8)	M_DCLKB25	M_DCLKB25	AL21	SB_CK[3]

(8)	M_DCLKB26	M_DCLKB26	AL21	SB_CK[3]
(8)	M_DCLKB27	M_DCLKB27	AL21	SB_CK[3]
(8)	M_DCLKB28	M_DCLKB28	AL21	SB_CK[3]

(8)	M_DCLKB29	M_DCLKB29	AL21	SB_CK[3]
(8)	M_DCLKB30	M_DCLKB30	AL21	SB_CK[3]
(8)	M_DCLKB31	M_DCLKB31	AL21	SB_CK[3]

(8)	M_DCLKB32	M_DCLKB32	AL21	SB_CK[3]
(8)	M_DCLKB33	M_DCLKB33	AL21	SB_CK[3]
(8)	M_DCLKB34	M_DCLKB34	AL21	SB_CK[3]

(8)	M_DCLKB35	M_DCLKB35	AL21	SB_CK[3]
(8)	M_DCLKB36	M_DCLKB36	AL21	SB_CK[3]
(8)	M_DCLKB37	M_DCLKB37	AL21	SB_CK[3]

(8)	M_DCLKB38	M_DCLKB38	AL21	SB_CK[3]
(8)	M_DCLKB39	M_DCLKB39	AL21	SB_CK[3]
(8)	M_DCLKB40	M_DCLKB40	AL21	SB_CK[3]

(8)	M_DCLKB41	M_DCLKB41	AL21	SB_CK[3]
(8)	M_DCLKB42	M_DCLKB42	AL21	SB_CK[3]
(8)	M_DCLKB43	M_DCLKB43	AL21	SB_CK[3]

(8)	M_DCLKB44	M_DCLKB44	AL21	SB_CK[3]
(8)	M_DCLKB45	M_DCLKB45	AL21	SB_CK[3]
(8)	M_DCLKB46	M_DCLKB46	AL21	SB_CK[3]

(8)	M_DCLKB47	M_DCLKB47	AL21	SB_CK[3]
(8)	M_DCLKB48	M_DCLKB48	AL21	SB_CK[3]
(8)	M_DCLKB49	M_DCLKB49	AL21	SB_CK[3]

(8)	M_DCLKB50	M_DCLKB50	AL21	SB_CK[3]
(8)	M_DCLKB51	M_DCLKB51	AL21	SB_CK[3]
(8)	M_DCLKB52	M_DCLKB52	AL21	SB_CK[3]

(8)	M_DCLKB53	M_DCLKB53	AL21	SB_CK[3]
(8)	M_DCLKB54	M_DCLKB54	AL21	SB_CK[3]
(8)	M_DCLKB55	M_DCLKB55	AL21	SB_CK[3]

(8)	M_DCLKB56	M_DCLKB56	AL21	SB_CK[3]
(8)	M_DCLKB57	M_DCLKB57	AL21	SB_CK[3]
(8)	M_DCLKB58	M_DCLKB58	AL21	SB_CK[3]

(8)	M_DCLKB59	M_DCLKB59	AL21	SB_CK[3]
(8)	M_DCLKB60	M_DCLKB60	AL21	SB_CK[3]
(8)	M_DCLKB61	M_DCLKB61	AL21	SB_CK[3]

(8)	M_DCLKB62	M_DCLKB62	AL21	SB_CK[3]
(8)	M_DCLKB63	M_DCLKB63	AL21	SB_CK[3]
(8)	M_DCLKB64	M_DCLKB64	AL21	SB_CK[3]

(8)	M_DCLKB65	M_DCLKB65	AL21	SB_CK[3]
(8)	M_DCLKB66	M_DCLKB66	AL21	SB_CK[3]
(8)	M_DCLKB67	M_DCLKB67	AL21	SB_CK[3]

(8)	M_DCLKB68	M_DCLKB68	AL21	SB_CK[3]
(8)	M_DCLKB69	M_DCLKB69	AL21	SB_CK[3]
(8)	M_DCLKB70	M_DCLKB70	AL21	SB_CK[3]

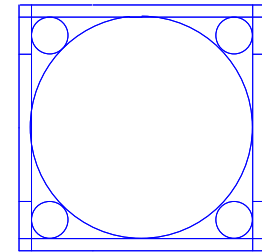
DDR_1

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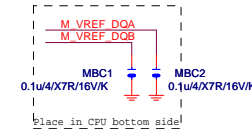
LGA1155[10SC1-F01155-01R]

LGA1155

ILM_BP/1156/BKNI



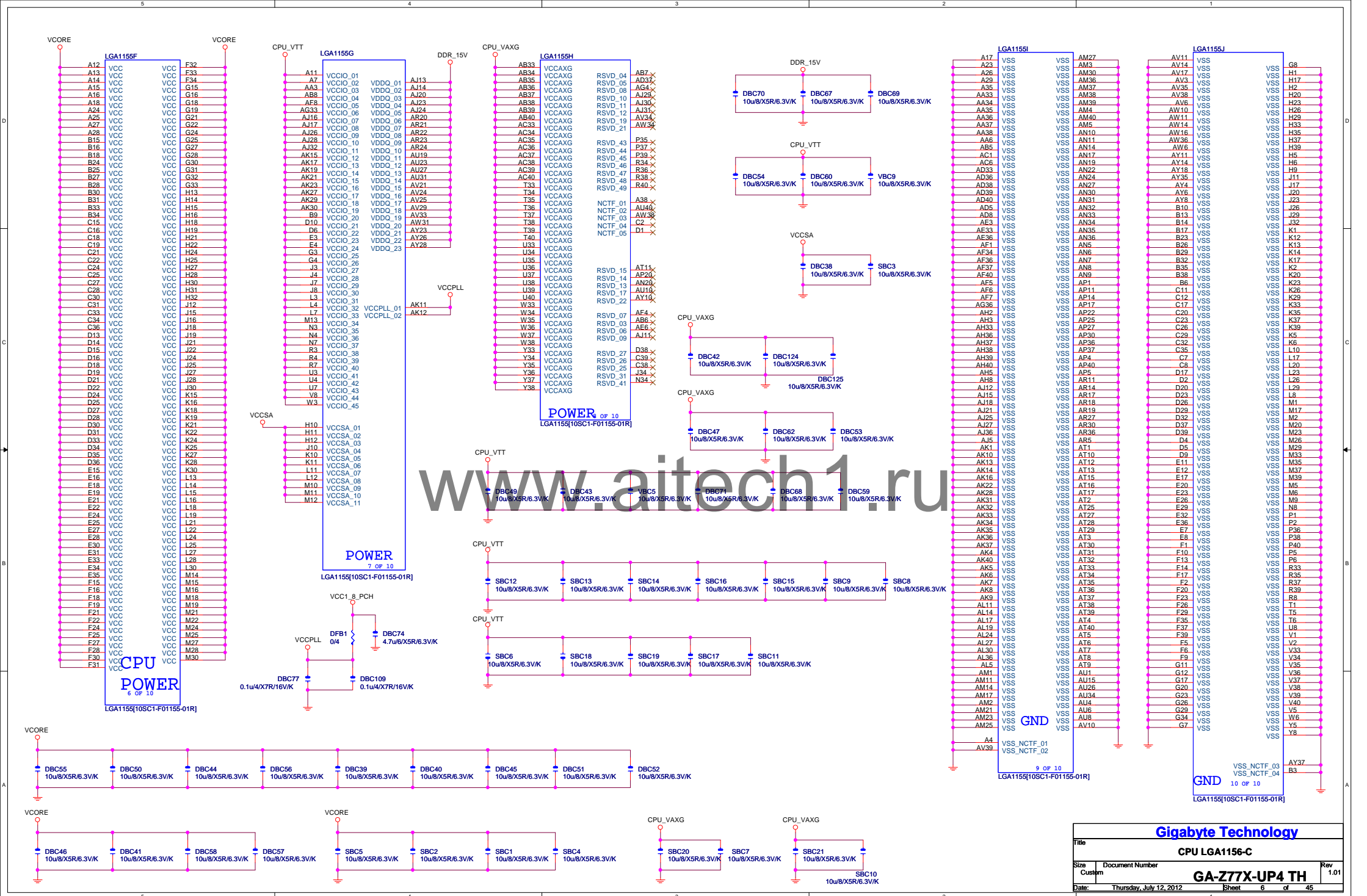
Need check the new CPU ME

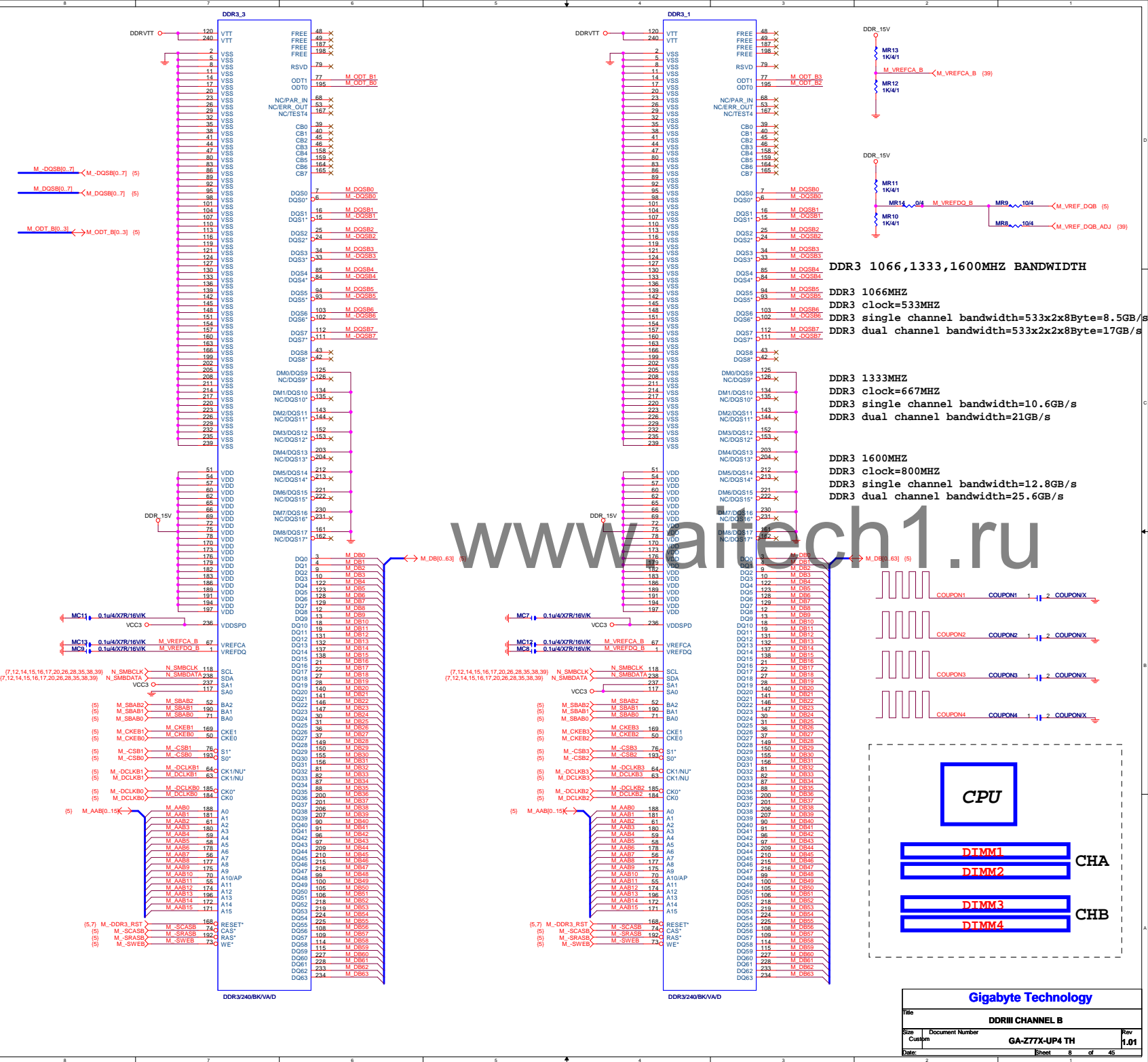


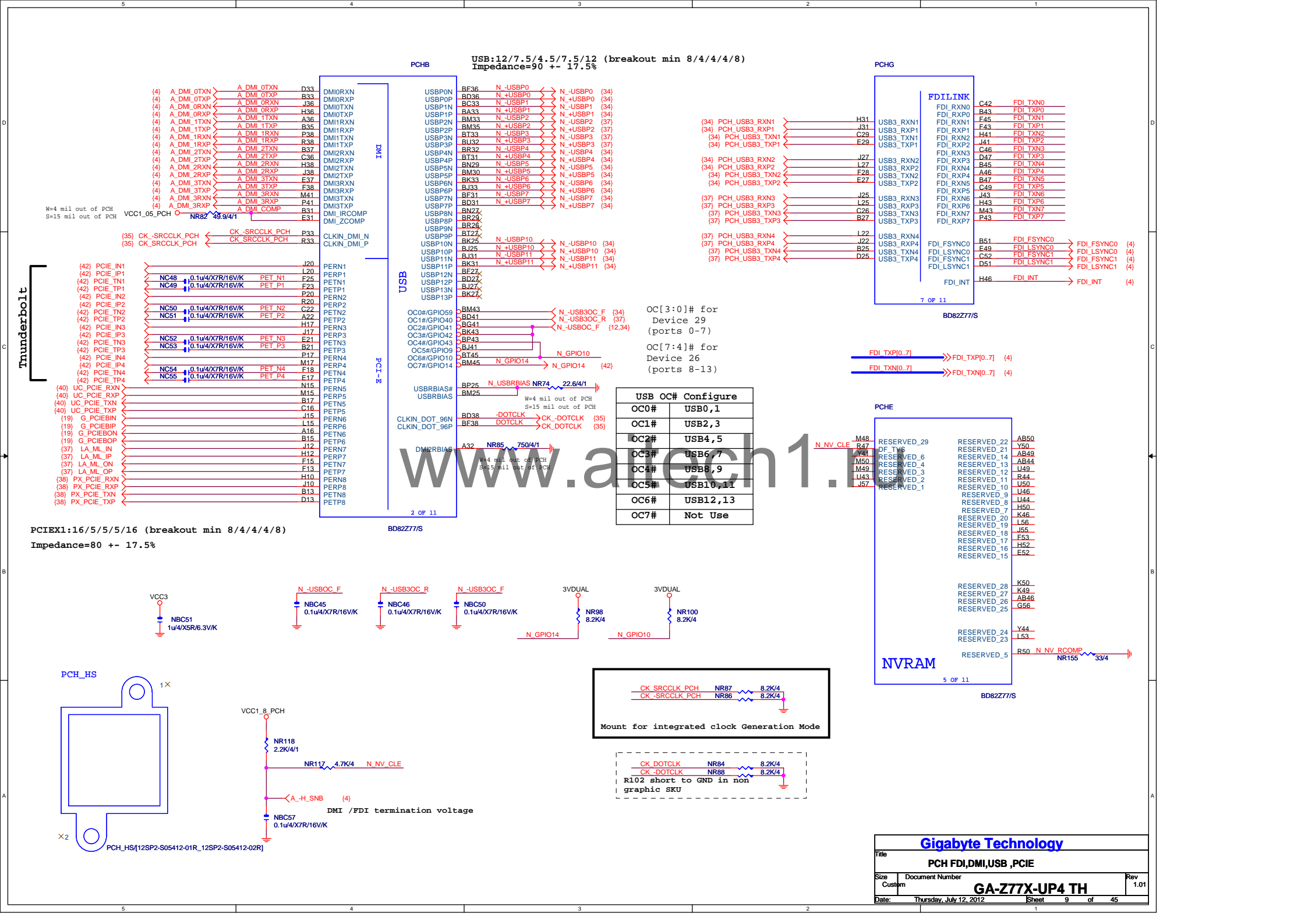
Gigabyte Technology

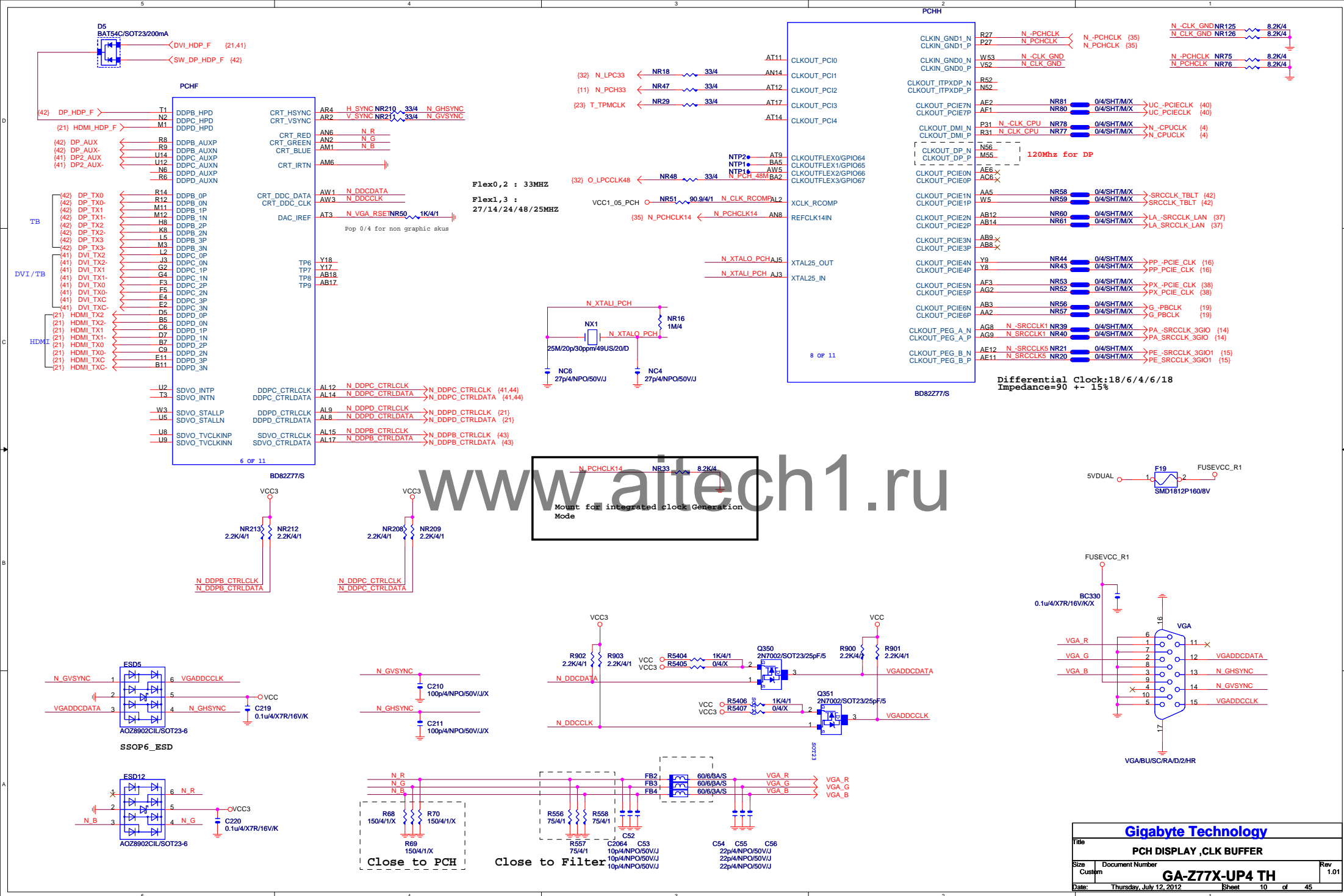
CPU LGA1156-B

Title	Document Number	Rev
Size	GA-Z77X-UP4 TH	1.01
Date	Thursday, July 12, 2012	Sheet 5 of 45

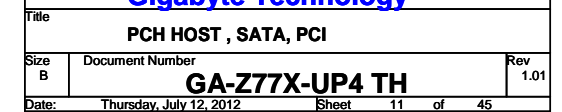


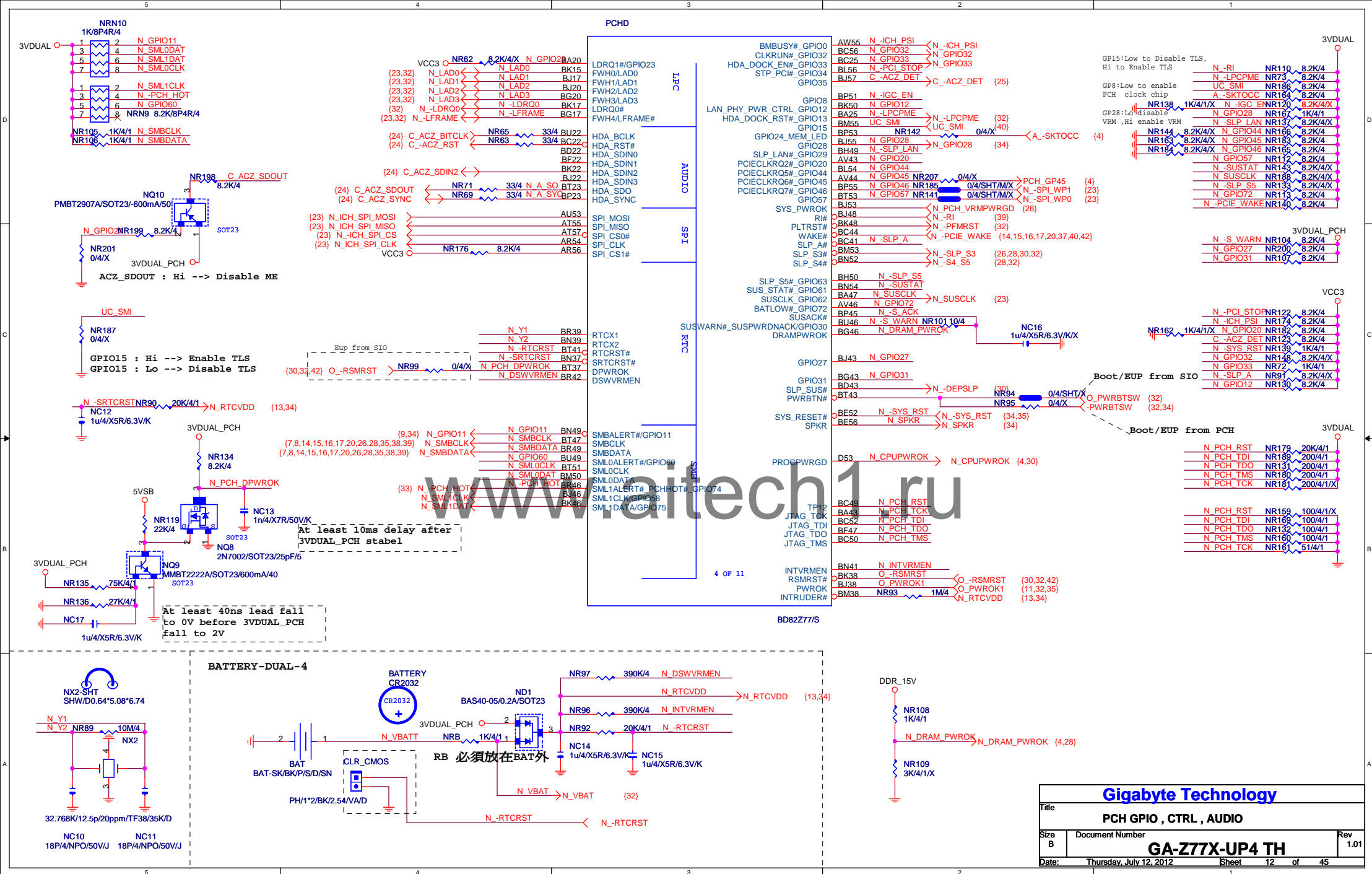


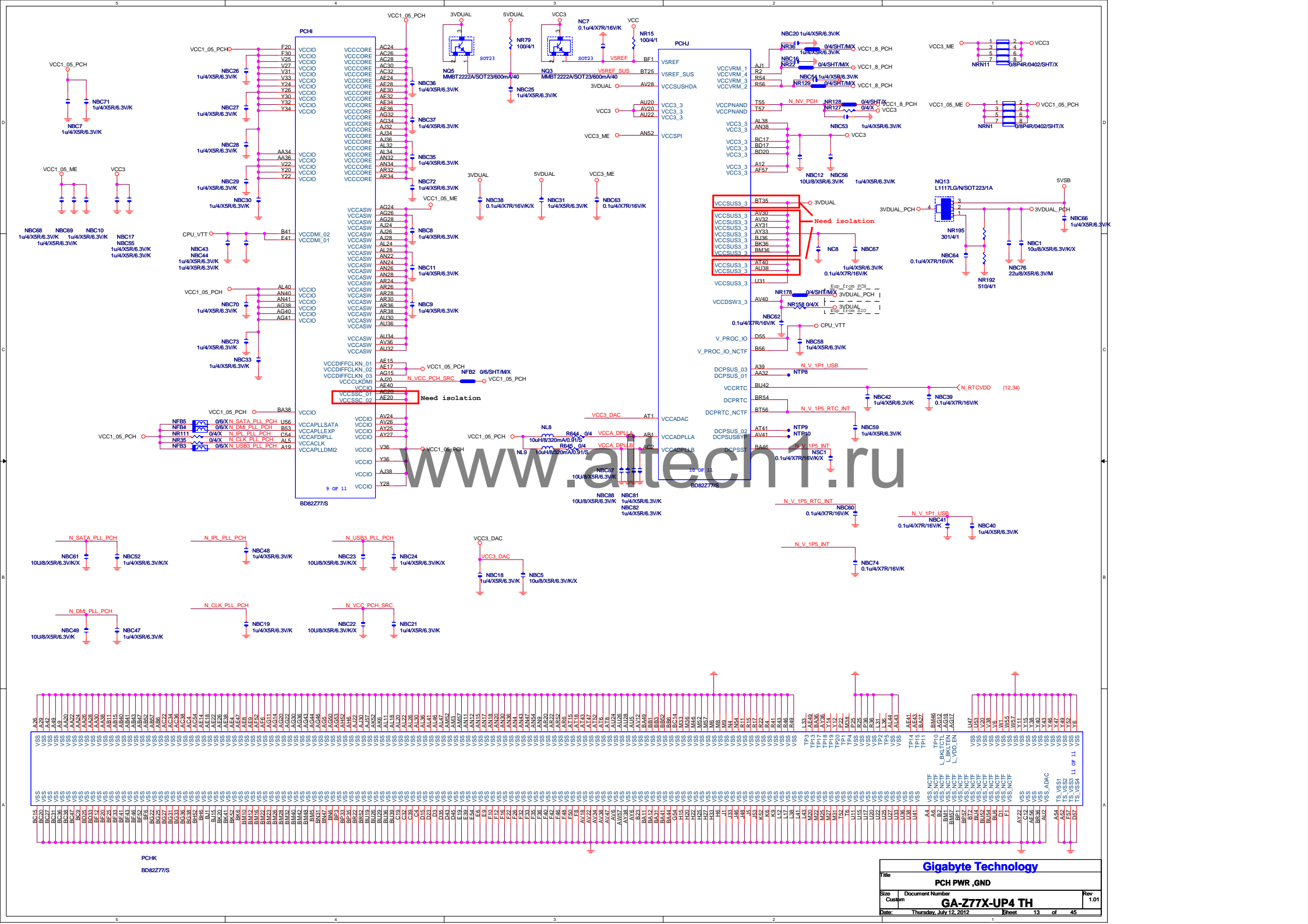


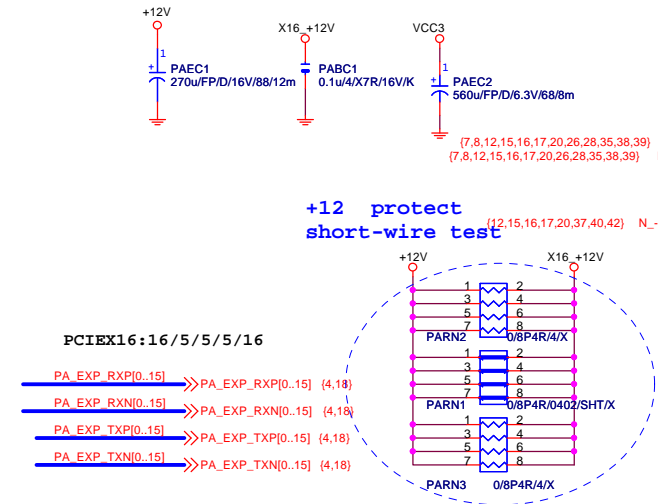


PCHC









PA EXP TXP0	PAC5	0.22u/4/X5R6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u/4/X5R6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u/4/X5R6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8	PAC20	0.22u/4/X5R6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8	PAC21	0.22u/4/X5R6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9	PAC22	0.22u/4/X5R6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9	PAC23	0.22u/4/X5R6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10	PAC24	0.22u/4/X5R6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10	PAC25	0.22u/4/X5R6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11	PAC26	0.22u/4/X5R6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11	PAC27	0.22u/4/X5R6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12	PAC28	0.22u/4/X5R6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12	PAC29	0.22u/4/X5R6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13	PAC30	0.22u/4/X5R6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13	PAC31	0.22u/4/X5R6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14	PAC32	0.22u/4/X5R6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14	PAC33	0.22u/4/X5R6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15	PAC34	0.22u/4/X5R6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15	PAC35	0.22u/4/X5R6.3V/K	PA EXP SW TXN15 C

PA EXP SW RXP8.15] >> PA_EXP_SW_RXP[8.15] (18)

PA EXP SW RXN8.15] >> PA_EXP_SW_RXN[8.15] (18)

PA EXP SW TXP8.15] >> PA_EXP_SW_TXP[8.15] (18)

PA EXP SW TXN8.15] >> PA_EXP_SW_TXN[8.15] (18)

PCI-E REV:1.1--> 2.5GHZ

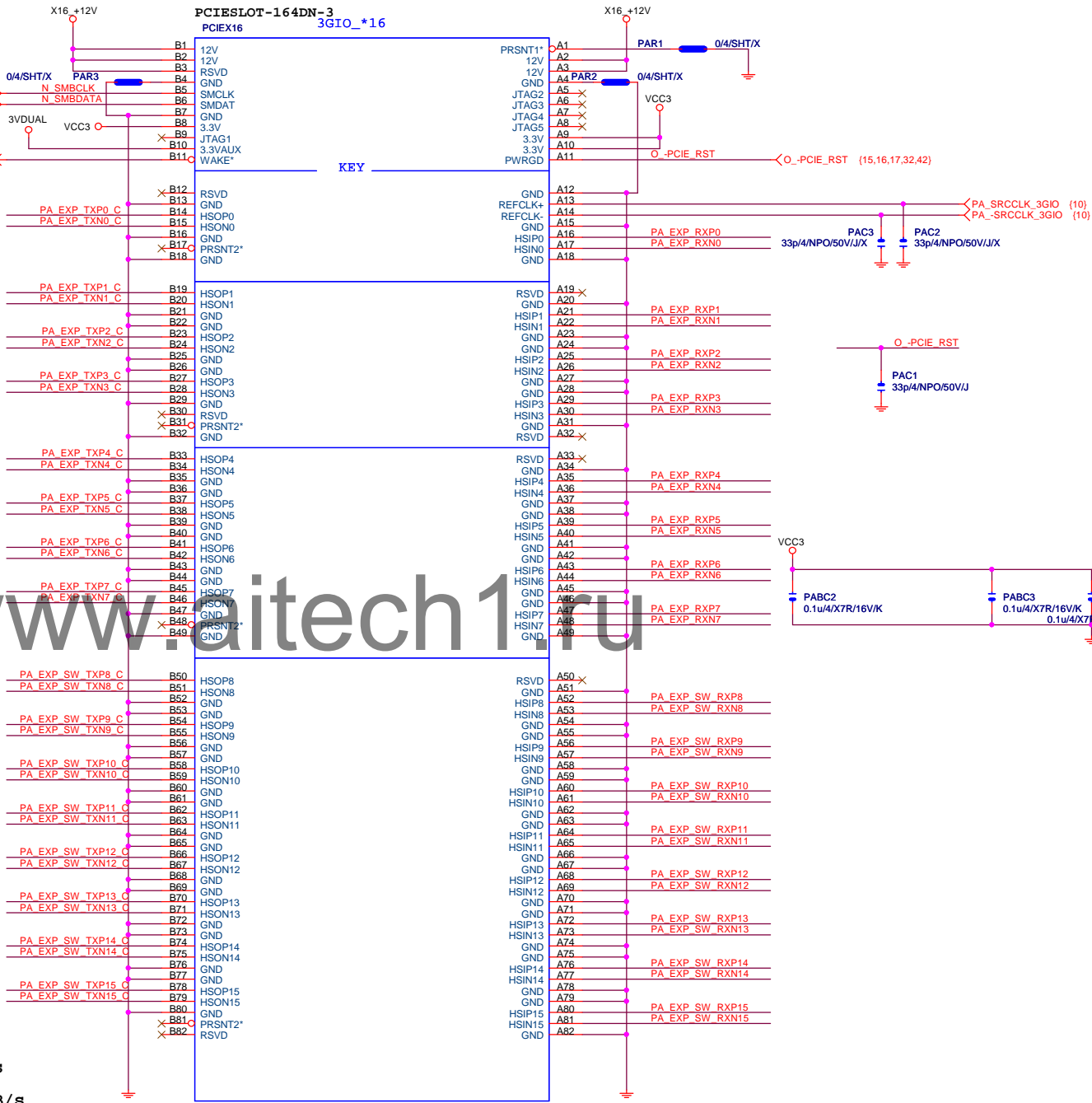
PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

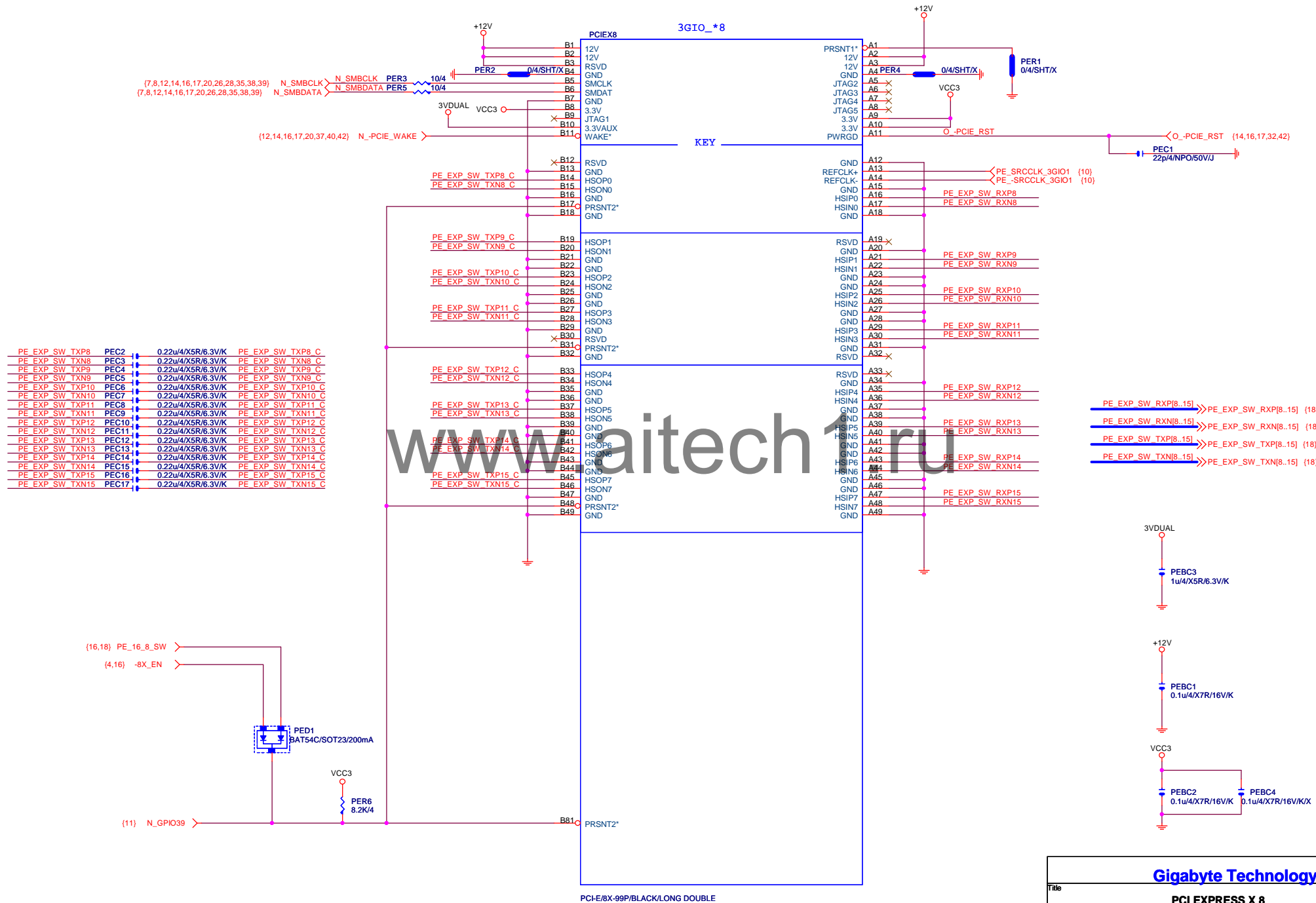
PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ



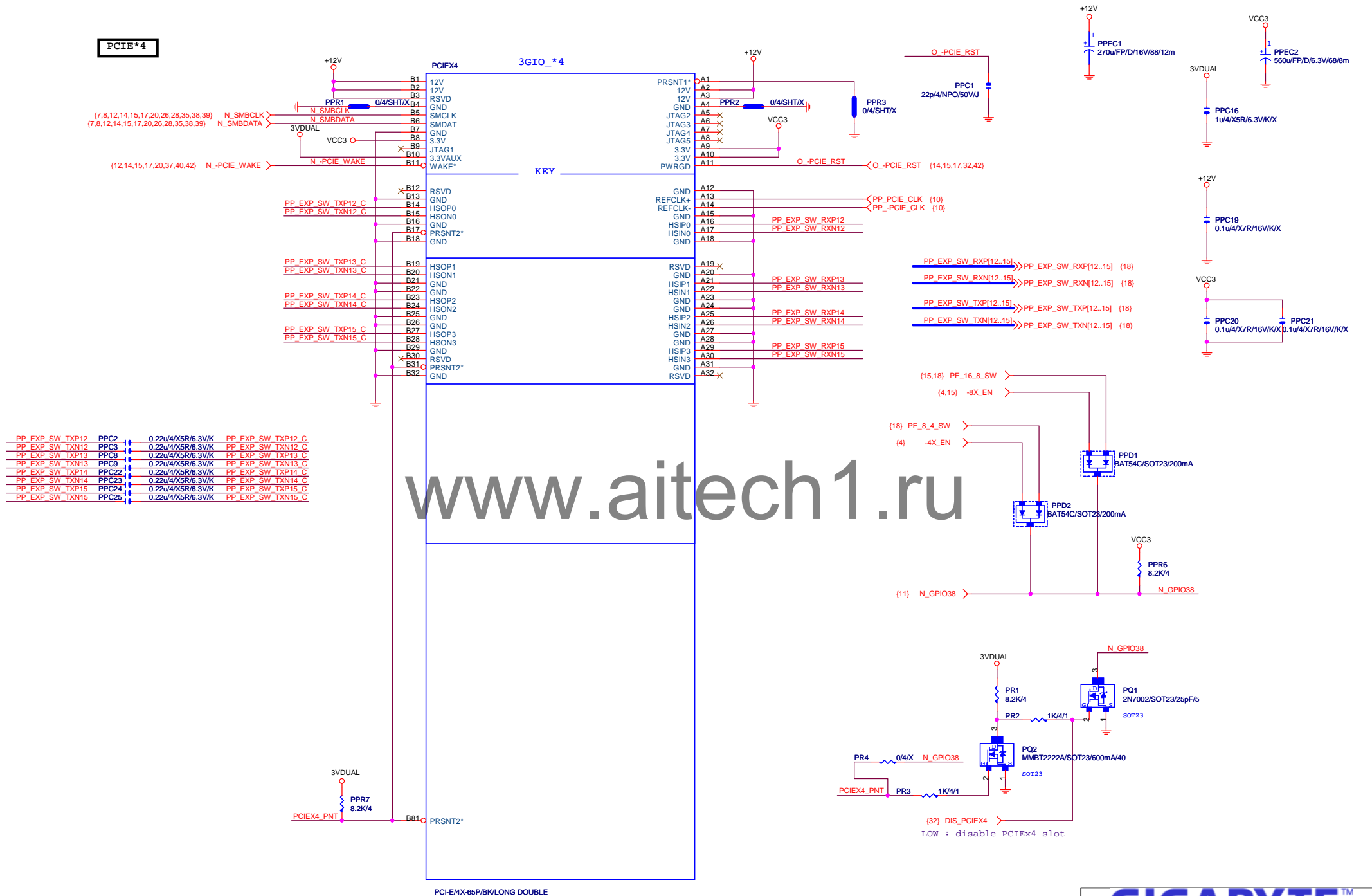
PCI-E/16X-164P/BK/LONG DOUBLE

Gigabyte Technology		
Title		
PCI EXPRESS X 16		
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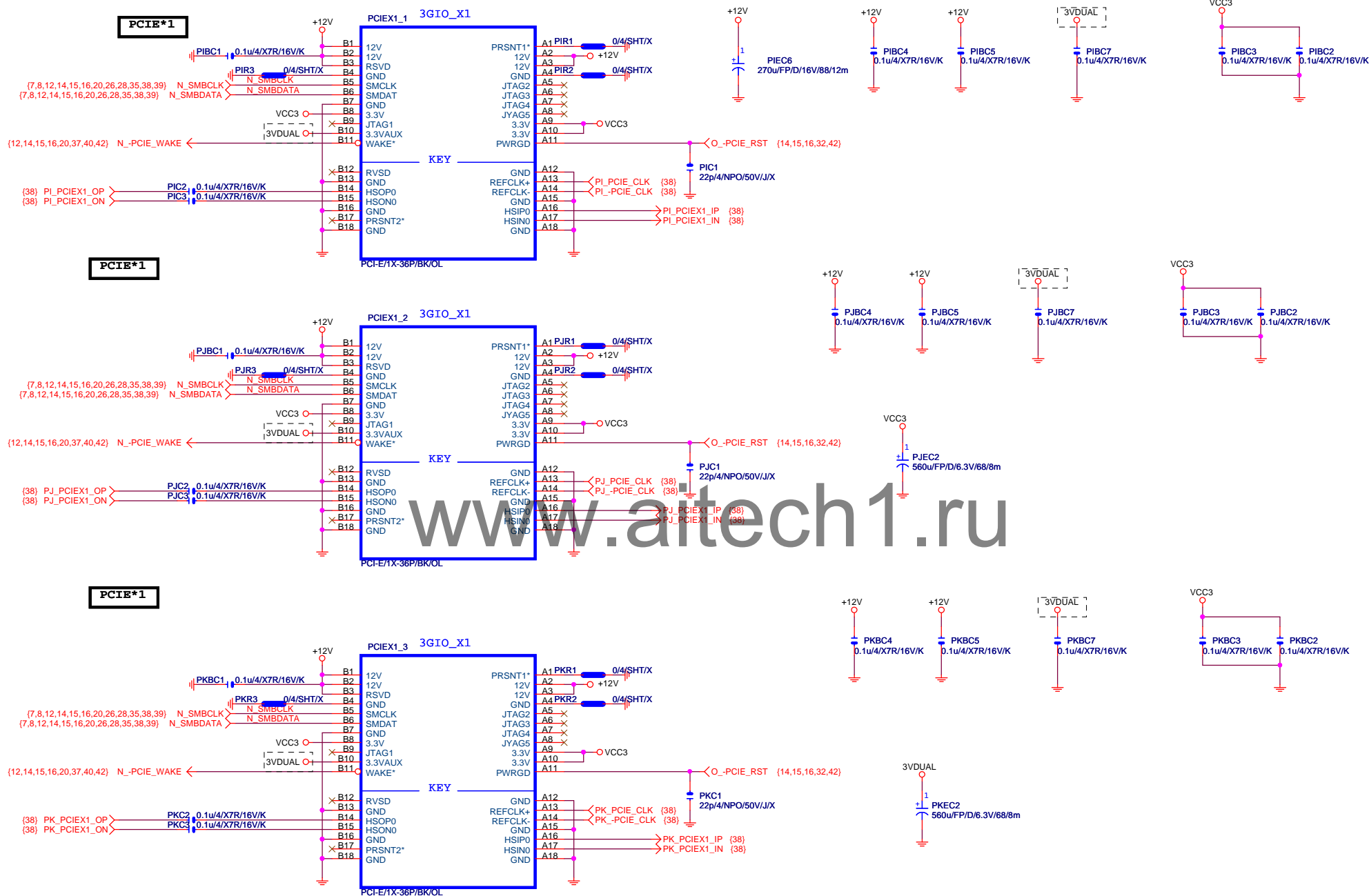


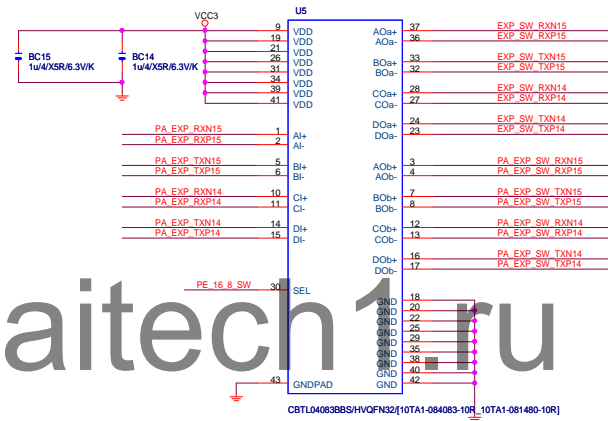
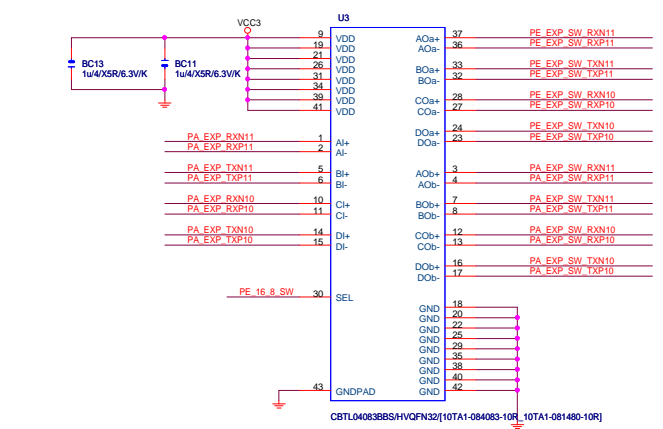
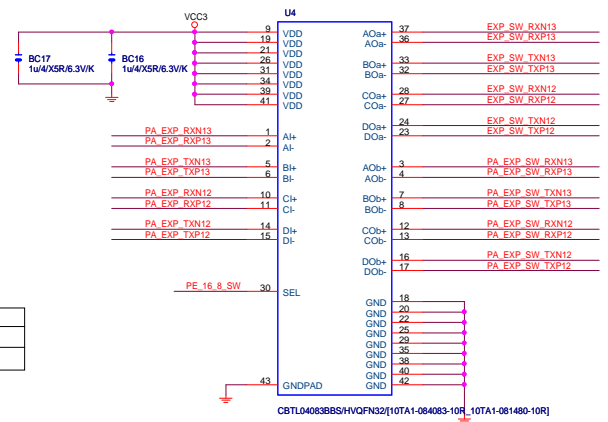
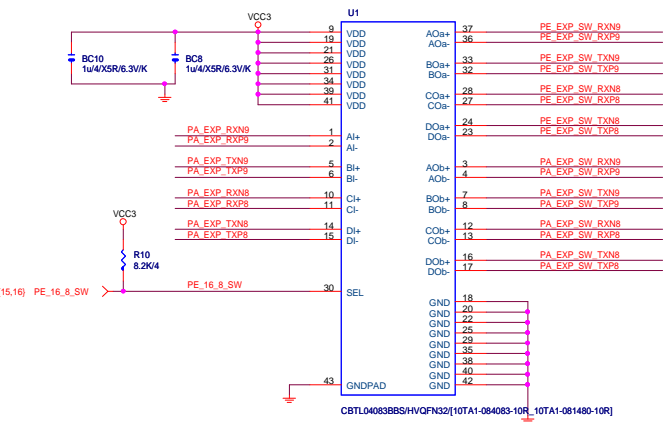
PCI-E/8X-99P/BLACK/LONG DOUBLE

PCIE*4

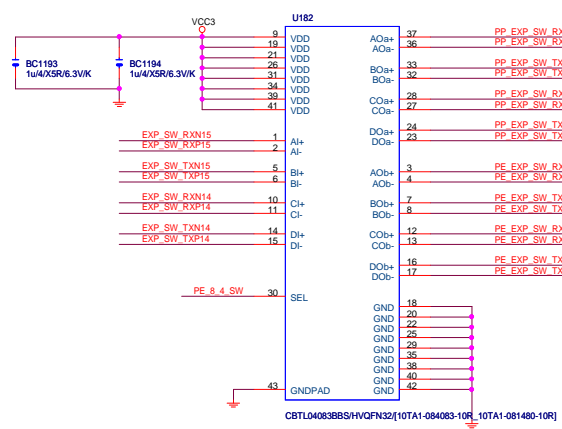
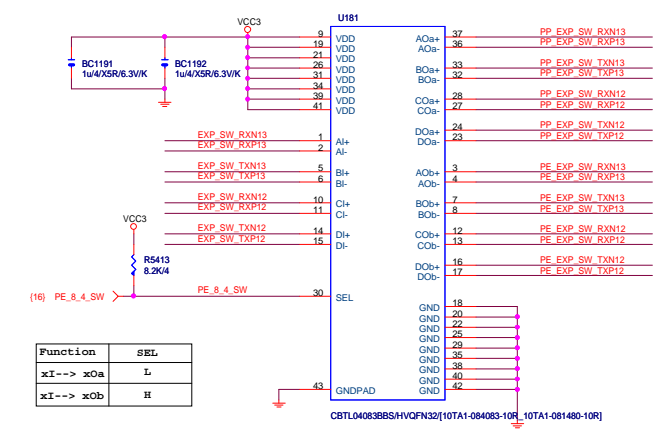


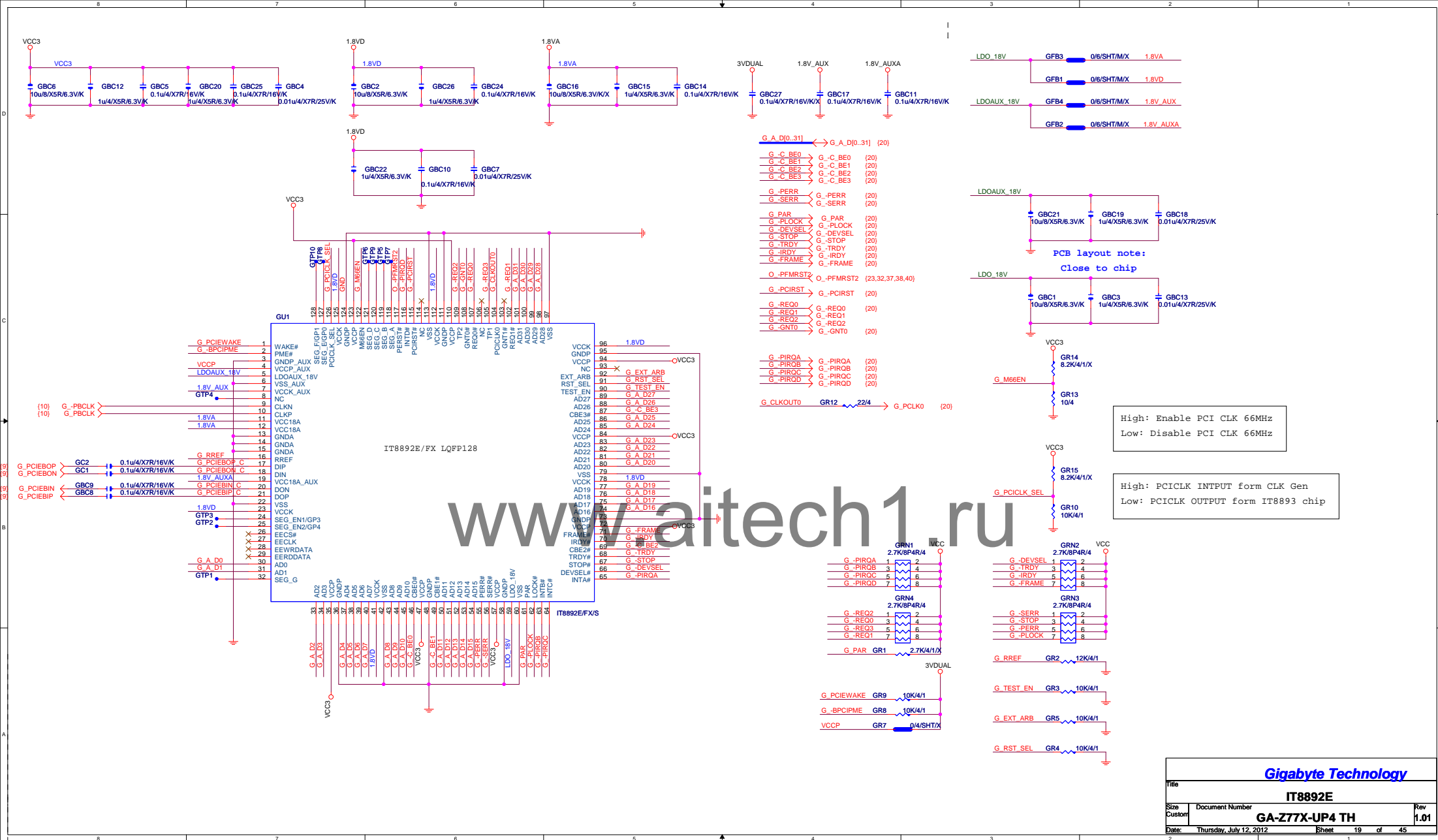
PCI-E/4X-65P/BK/LONG DOUBLE

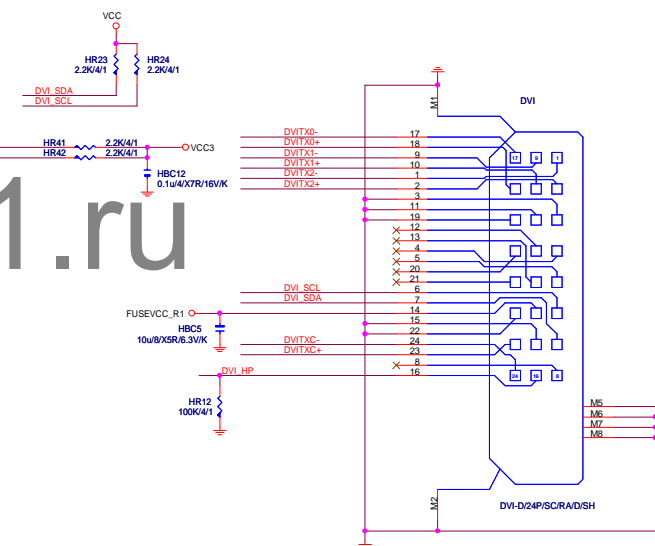
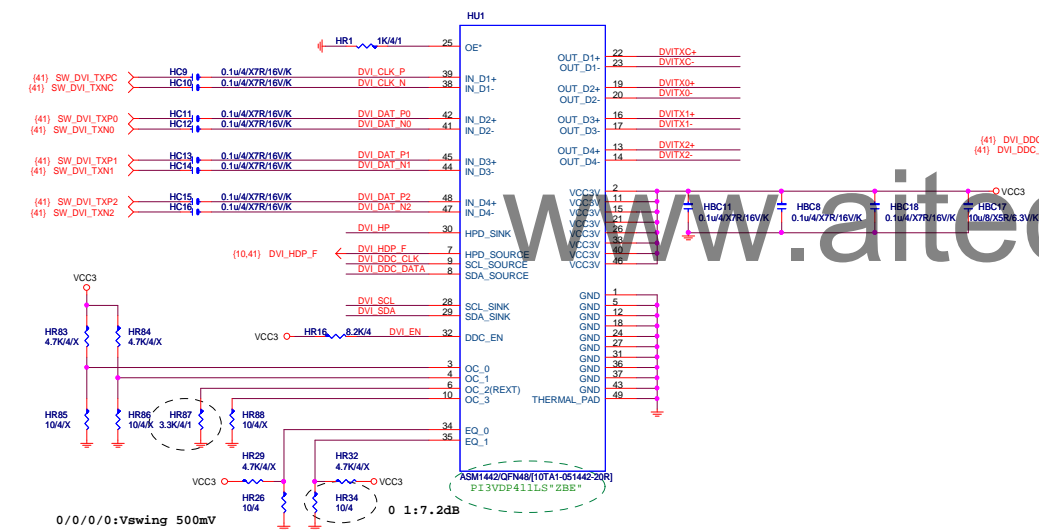
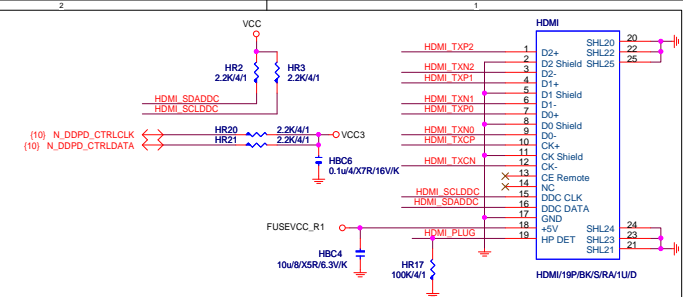
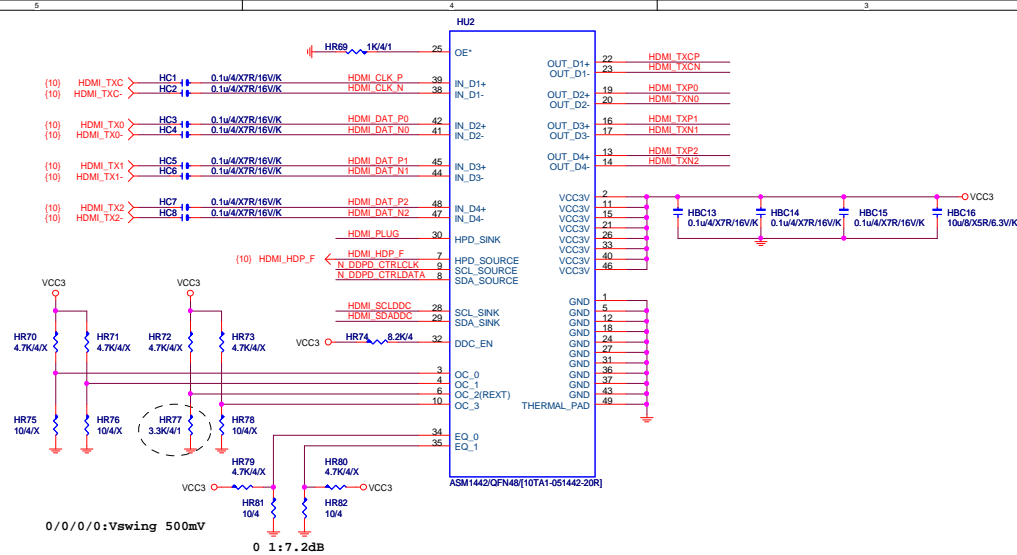


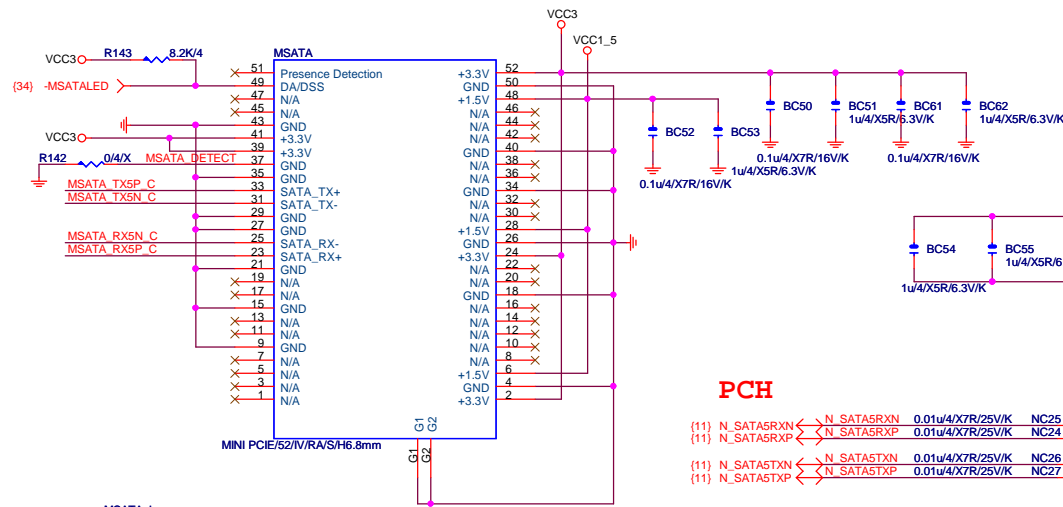


- PA_EXP_RXP0..15 >>> PA_EXP_RXP0..15 (4,14)
- PA_EXP_RXN0..15 >>> PA_EXP_RXN0..15 (4,14)
- PA_EXP_TXP0..15 >>> PA_EXP_TXP0..15 (4,14)
- PA_EXP_TXN0..15 >>> PA_EXP_TXN0..15 (4,14)
- PA_EXP_SW_RXP8..15 >>> PA_EXP_SW_RXP8..15 (14)
- PA_EXP_SW_RXN8..15 >>> PA_EXP_SW_RXN8..15 (14)
- PA_EXP_SW_TXP8..15 >>> PA_EXP_SW_TXP8..15 (14)
- PA_EXP_SW_TXN8..15 >>> PA_EXP_SW_TXN8..15 (14)
- PE_EXP_SW_RXP8..15 >>> PE_EXP_SW_RXP8..15 (15)
- PE_EXP_SW_RXN8..15 >>> PE_EXP_SW_RXN8..15 (15)
- PE_EXP_SW_TXP8..15 >>> PE_EXP_SW_TXP8..15 (15)
- PE_EXP_SW_TXN8..15 >>> PE_EXP_SW_TXN8..15 (15)
- PP_EXP_SW_RXP12..15 >>> PP_EXP_SW_RXP12..15 (16)
- PP_EXP_SW_RXN12..15 >>> PP_EXP_SW_RXN12..15 (16)
- PP_EXP_SW_TXP12..15 >>> PP_EXP_SW_TXP12..15 (16)
- PP_EXP_SW_TXN12..15 >>> PP_EXP_SW_TXN12..15 (16)

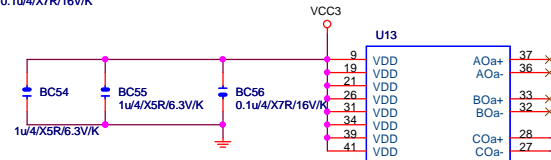






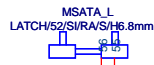


N SATA5RXN C R134 0/4/X N SATA5RXNC
 N SATA5RXP C R136 0/4/X N SATA5RXPNC
 N SATA5TXN C R137 0/4/X N SATA5TXNC
 N SATA5TXP C R139 0/4/X N SATA5TXPC
FIX PCH-SATA --> SATA5
R請放在U13背面



PCH

(11) N_SATA5RXN <--> N_SATA5RXN 0.01u/4/X7R/25V/K NC25 N_SATA5RXN C 10
 (11) N_SATA5RXP <--> N_SATA5RXP 0.01u/4/X7R/25V/K NC24 N_SATA5RXP C 11
 (11) N_SATA5TXN <--> N_SATA5TXN 0.01u/4/X7R/25V/K NC26 N_SATA5TXN C 14
 (11) N_SATA5TXP <--> N_SATA5TXP 0.01u/4/X7R/25V/K NC27 N_SATA5TXP C 15



MSATA L LATCH/52/SI/RA/SH/6.8mm

Q46 L1117LG/N/SOT223/1A

VCC3

VCC1_5

BC57 1u/4/X5R/6.3V/K

R140 100/4/1

BC58 1u/4/X5R/6.3V/K

R141 21/4/1 22u/8/X5R/6.3V/M

BC60 0.1u/4/X7R/16V/K

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MSATA_SW

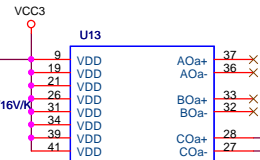


MSATA_DETECT

R135 8.2K/4

R138 22K/4

Q45 MMBT2222A/SOT23/600mA/40 SOT23



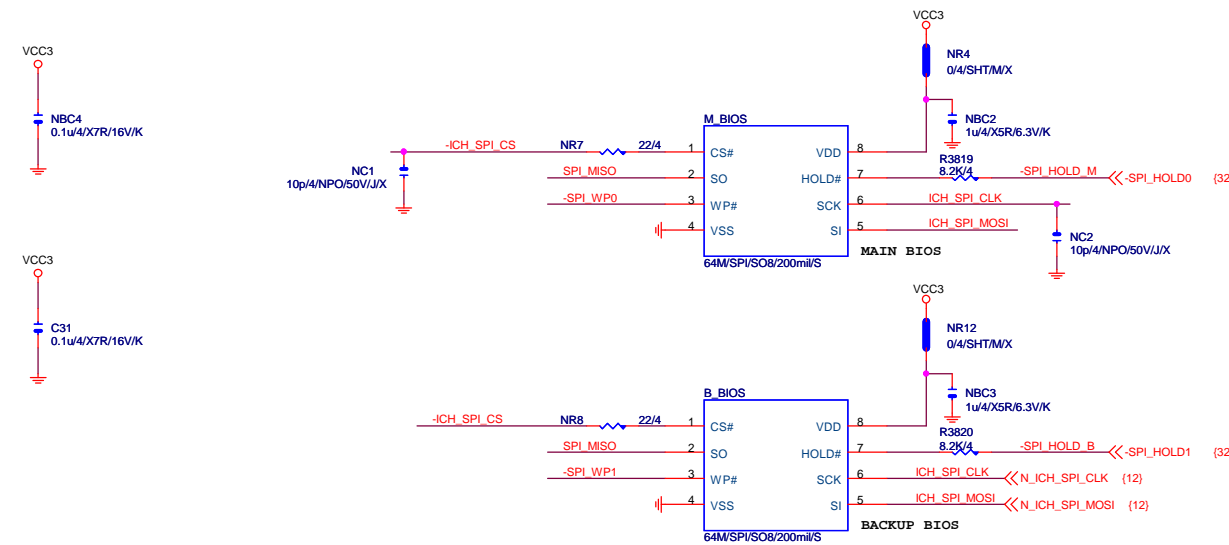
SATA2 port5

mSATA

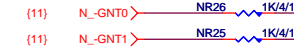
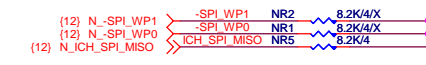
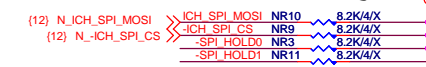
Function	SEL
xI--> xOa	L
xI--> xOb	H

GIGABYTE™

Title	mSATA Conn		
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MOSI For DMI RX Termination Voltage



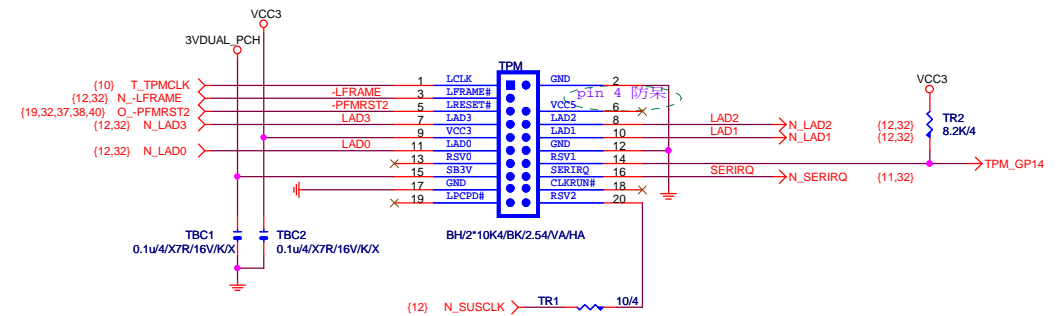
Default int pull up



BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

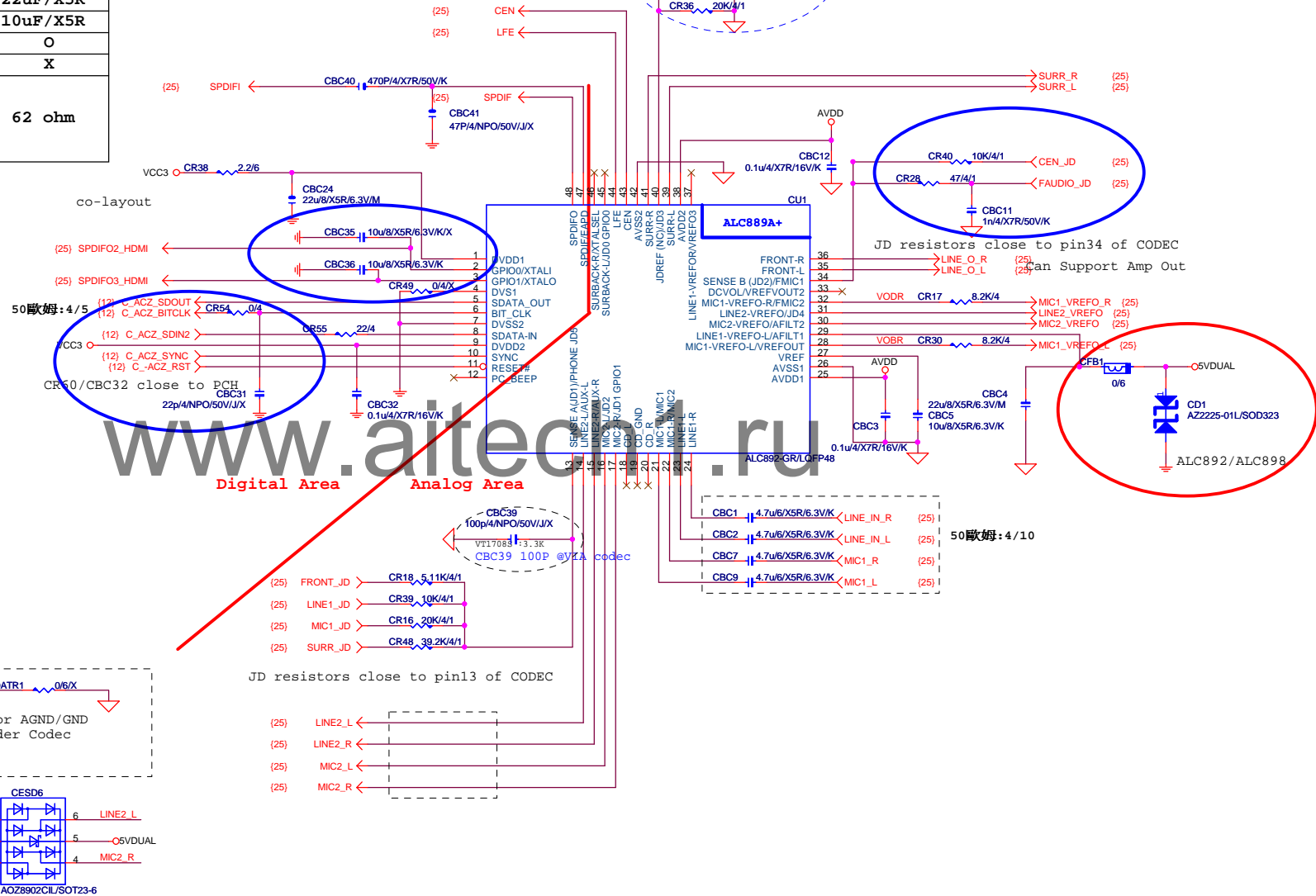
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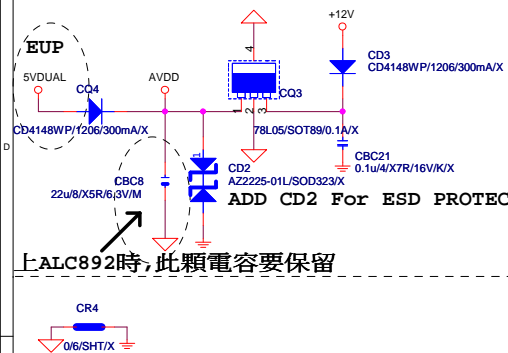
Gigabyte Technology

Title				BIOS	
Size	Custom	Document Number	GA-Z77X-UP4 TH		Rev
				1.01	
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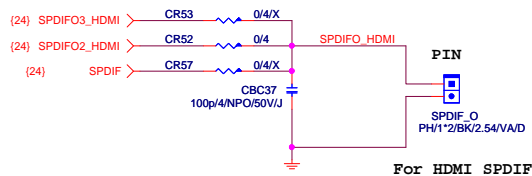
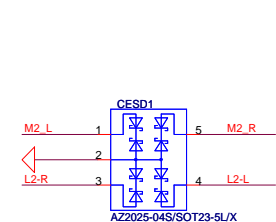
	ALC889	ALC889B	ALC898/ALC892
CR49	O	O	X
CBC36	X	X	10uF/X5R
CBC35	X	10uF/X5R	X
CR52	O	X	O
CR53	X	O	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC7/CBC9/CBC20/CBC15	10uF/X5R	10uF/X5R	10uF/X5R
CFB1/CD1/CBC4	X	X	O
CD2/CD3/CQ3/CQ4	O	O	X
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47/ CR2/CR11/CR14/CR24	62 ohm	62 ohm	62 ohm



CODEC POWER/EMI PAD

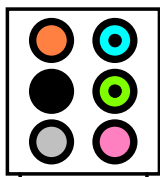


上ALC892時,此顆電容要保留

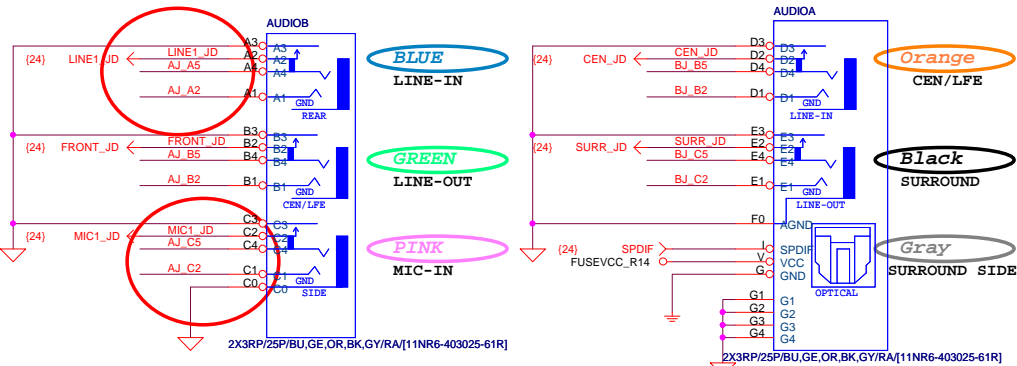
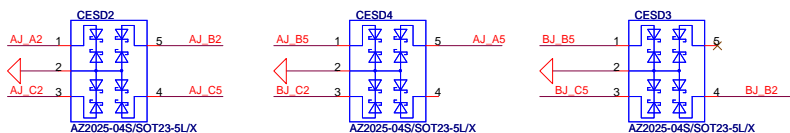


AZALIA JACK

BTX AZALIA CONNECTOR



11NR6-403007-21R



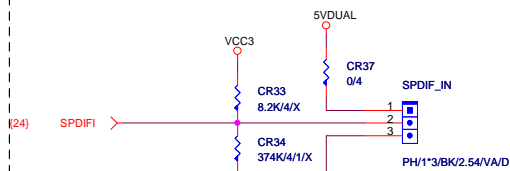
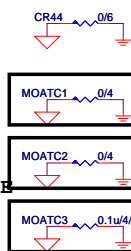
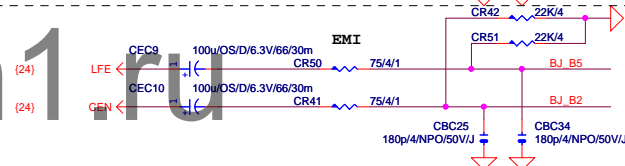
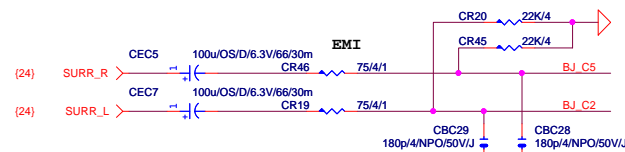
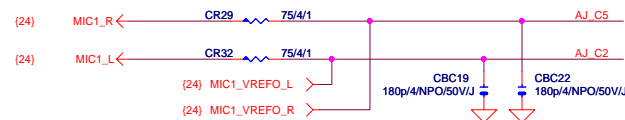
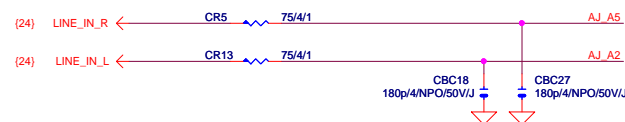
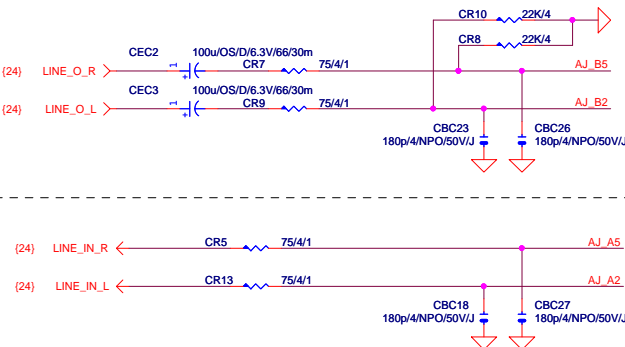
LINE-OUT

Audio jack --> USB

Near Audio jack|left

```
Codec --> Audio jack
```

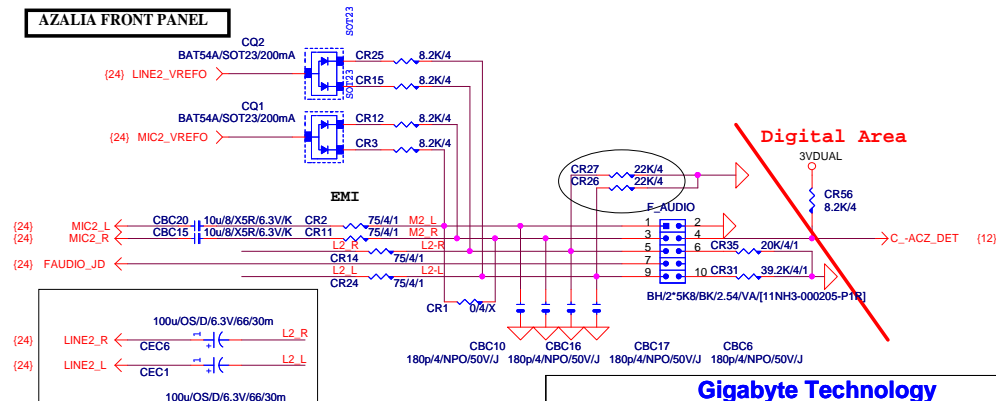
F_AUDIO

**MIC-IN**

CEN/LFE

SURR BACK

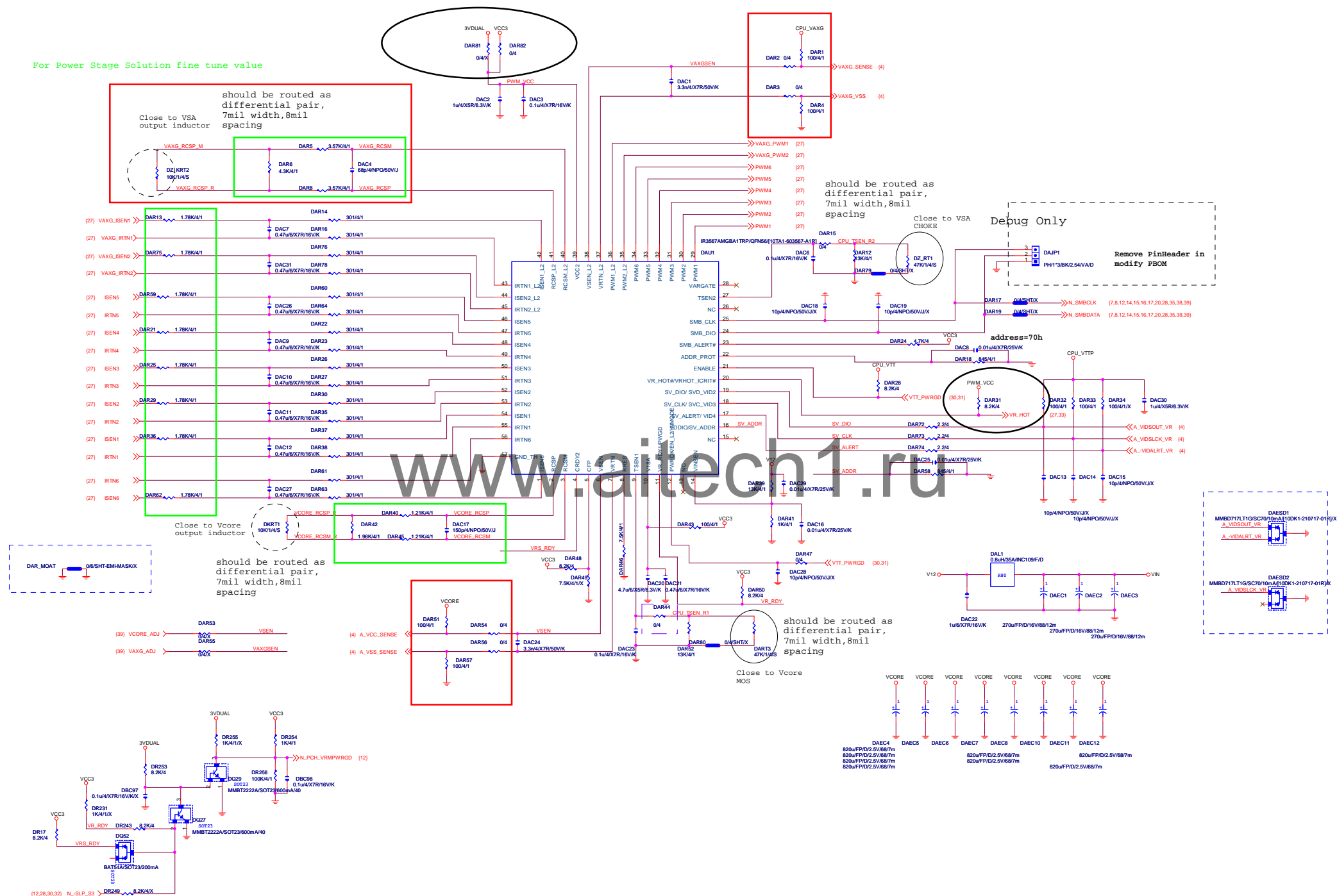
AZALIA FRONT PANEL



Digital Area

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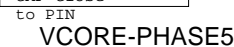
For Power Stage Solution fine tune value



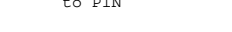
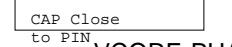
(3553 / 3550 co-lay)



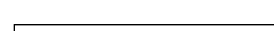
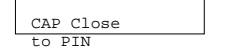
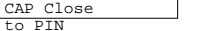
VCORE-PHASE5

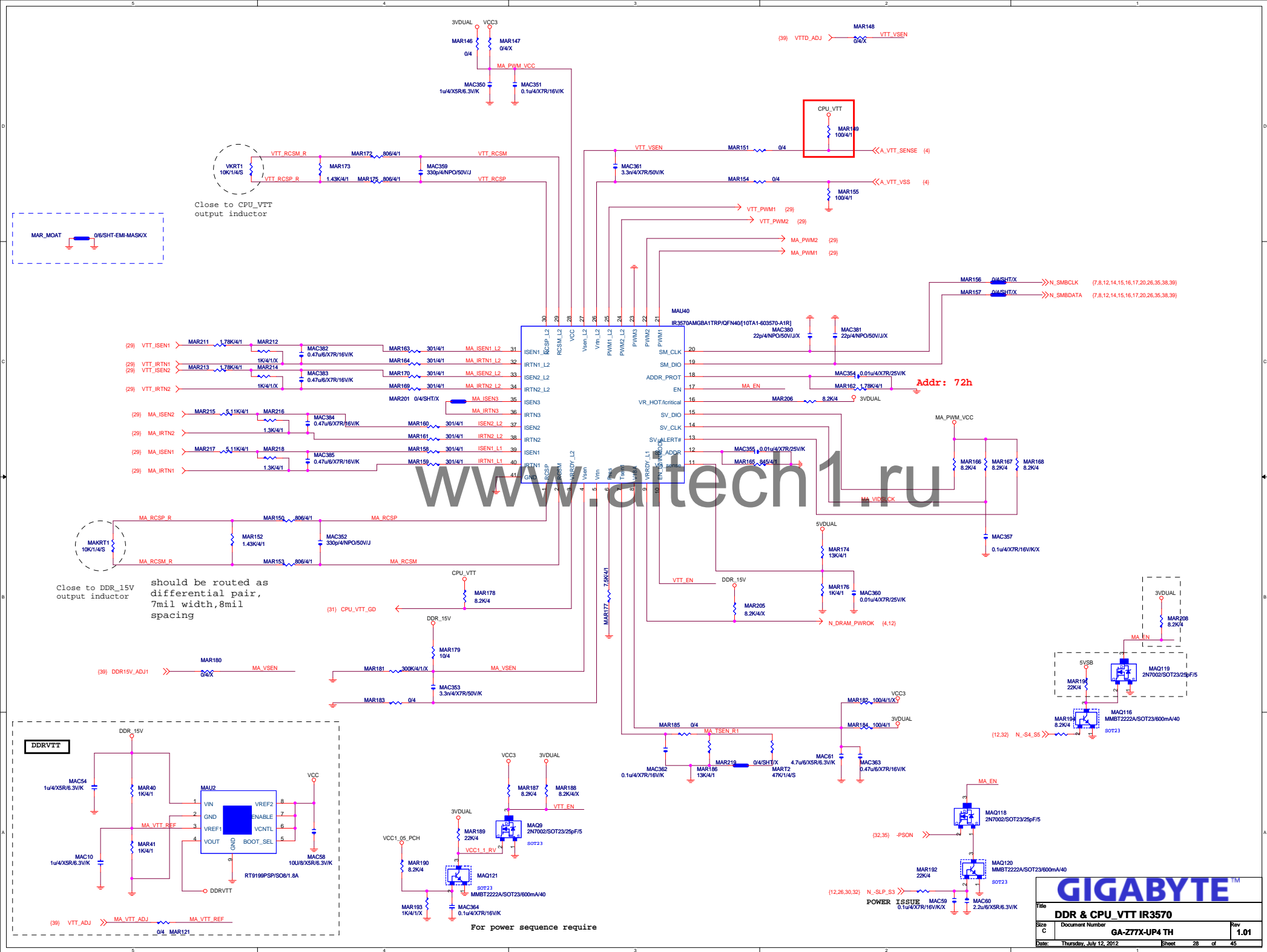


VCORE-PHASE6

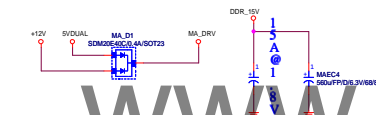
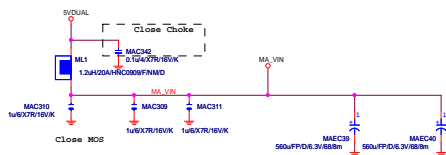
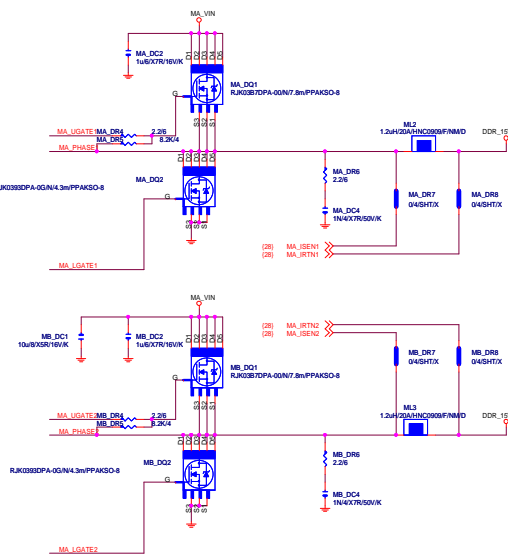
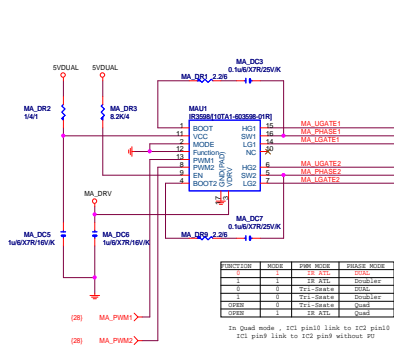


VAXG Phase

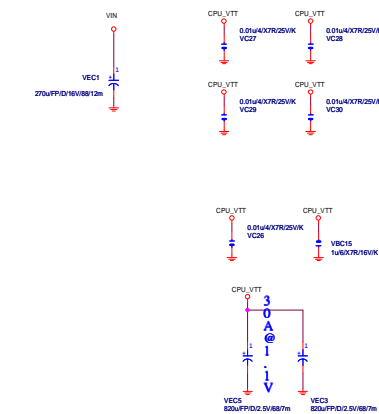
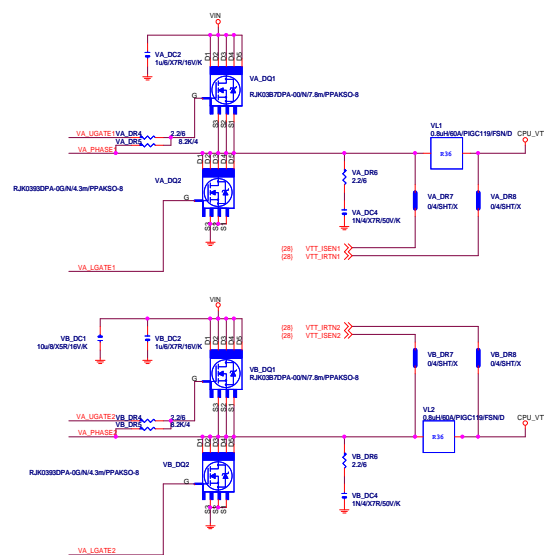
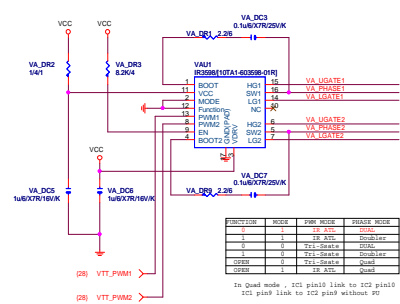


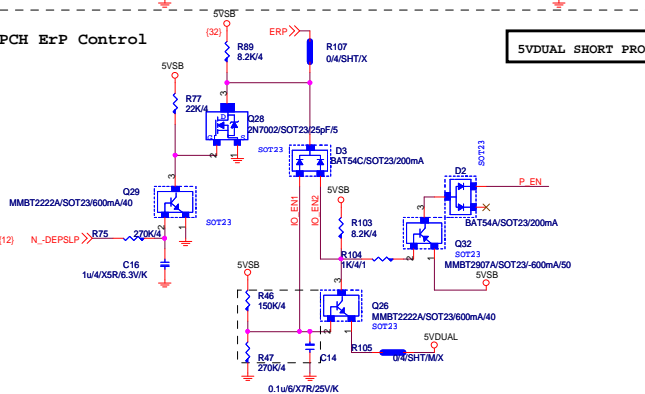
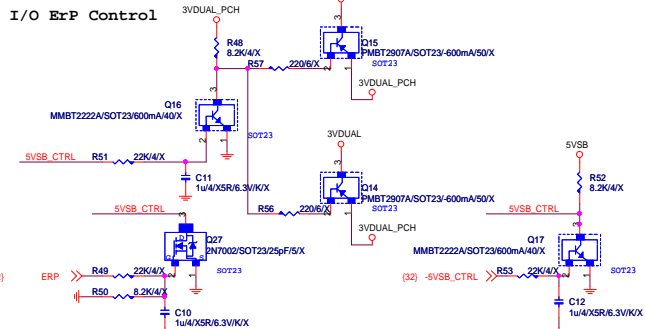
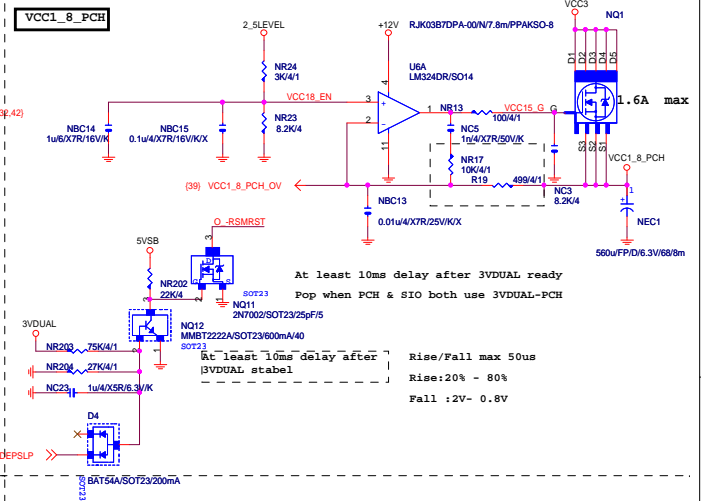
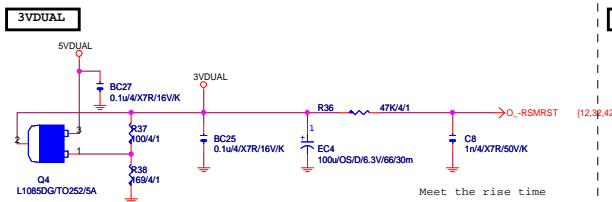
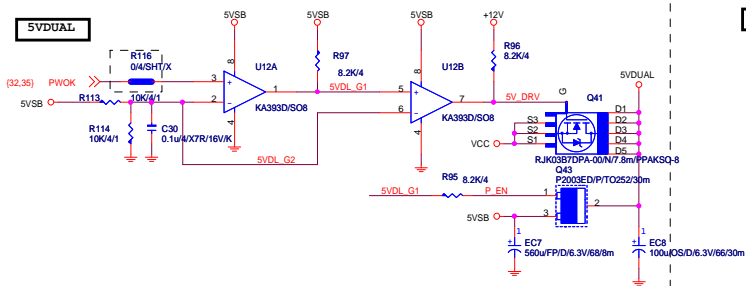


DDR_15V

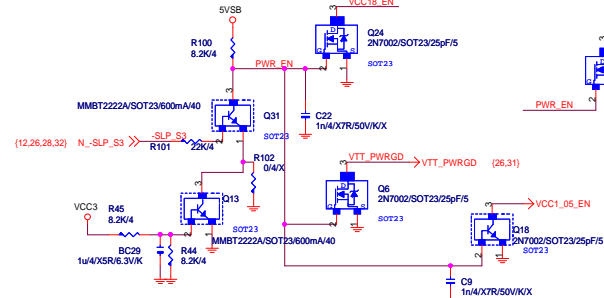
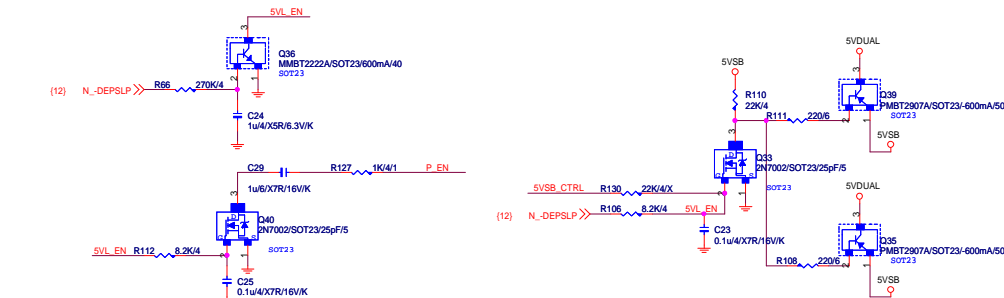
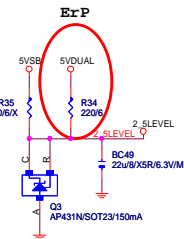


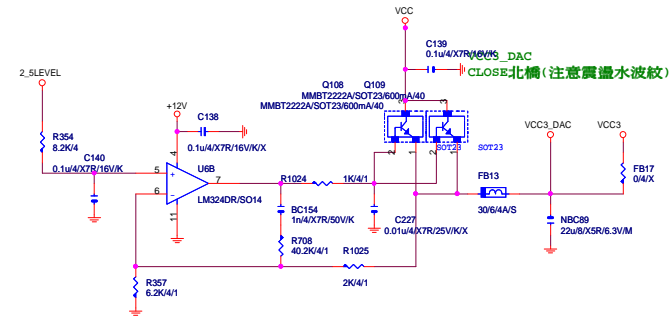
CPU_VTT



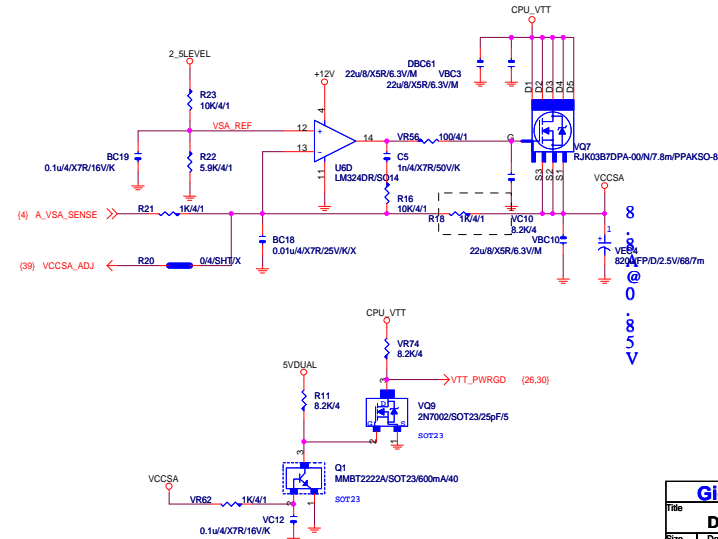


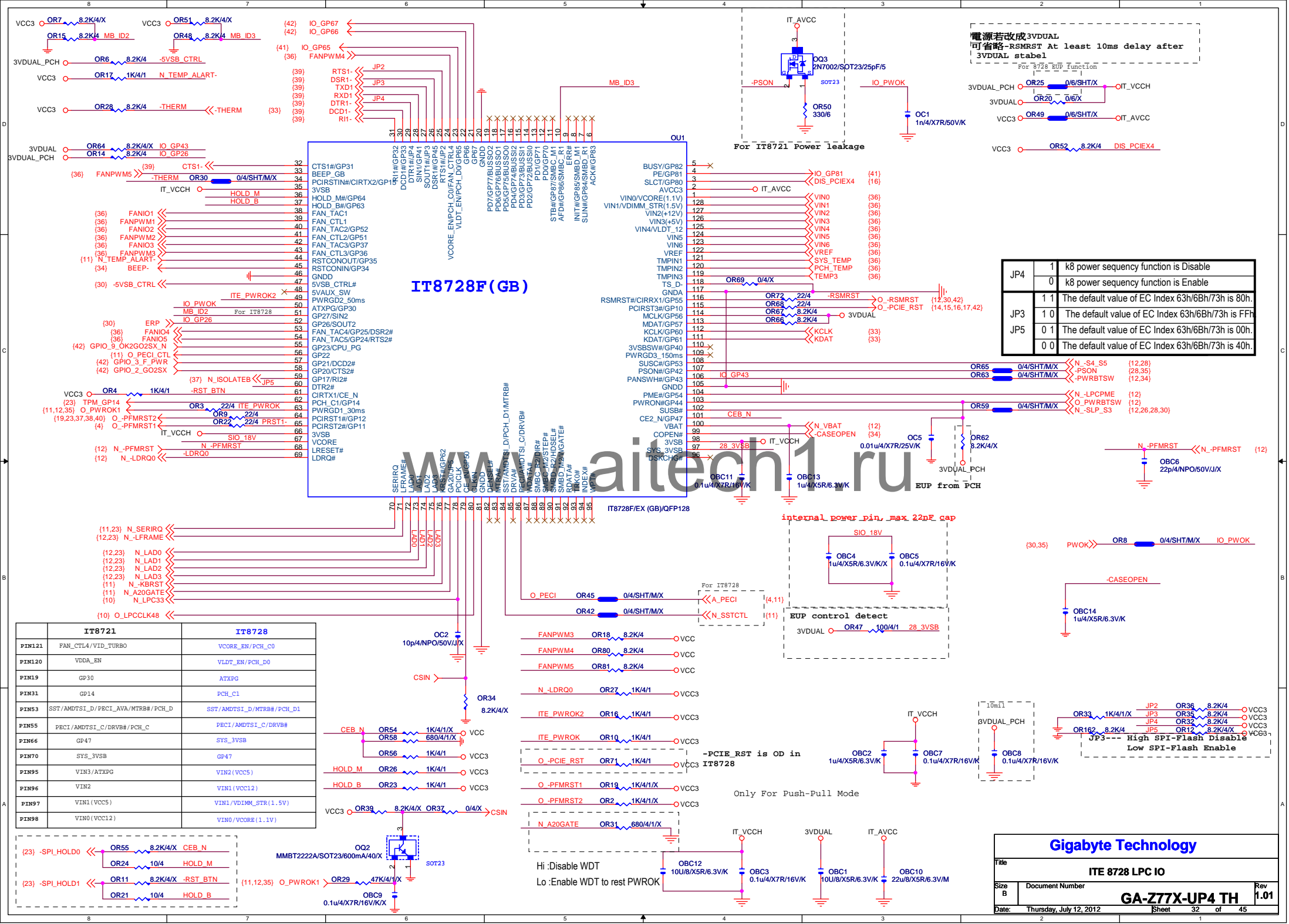
5VDUAL SHORT PROTECT

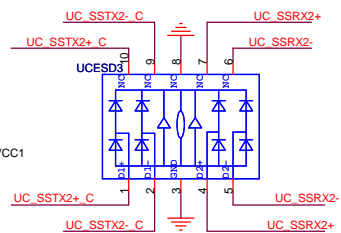
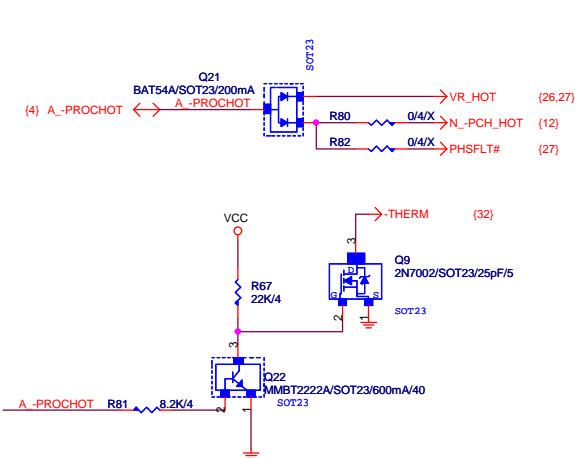


$$(3.3V/70mA+360\mu A)$$


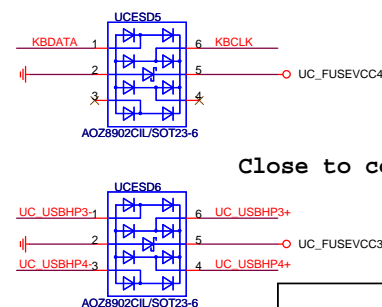
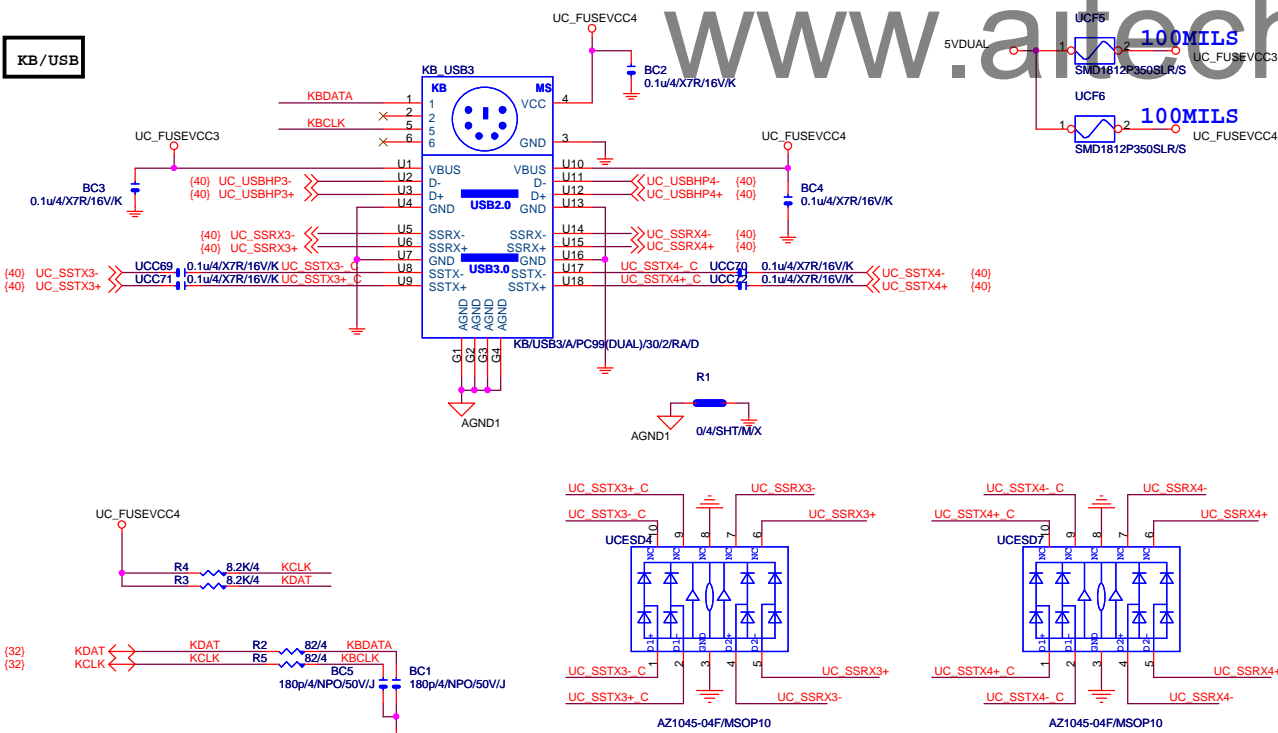
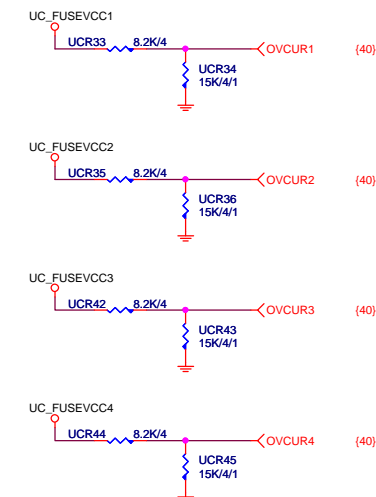
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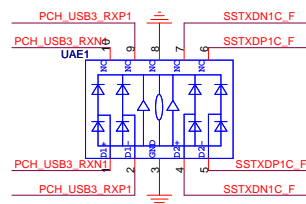
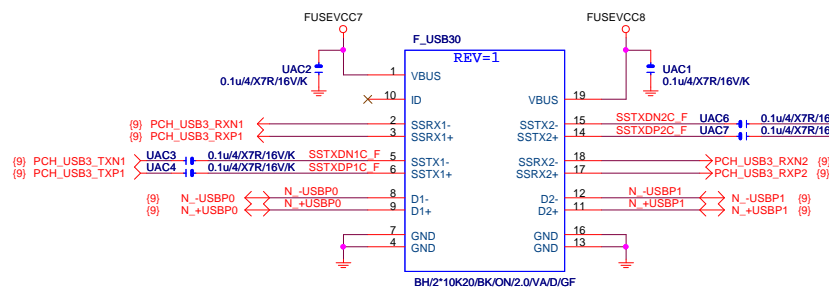


Close to connector



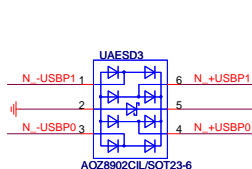
Close to connector

<h1 style="text-align: center; color: blue;">Gigabyte Technology</h1>				
Title				
USB3_ESATA / KB_USB3				
Size	Document Number			Rev
Custom	GA-Z77X-UP4 TH			1.0
Date:	Thursday, July 12, 2012	Sheet	33 of 45	

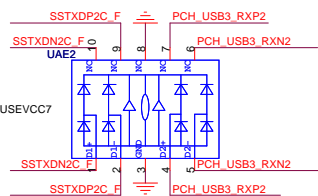


AZ1045-04F/MSOP10

Close to connector

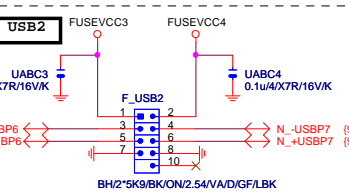
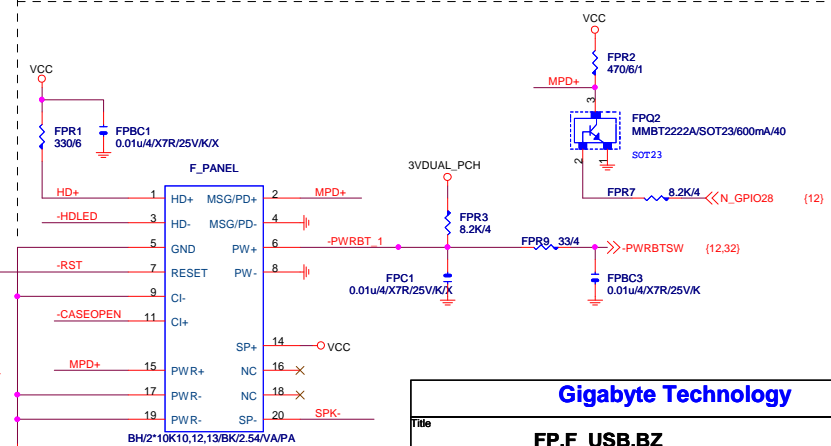
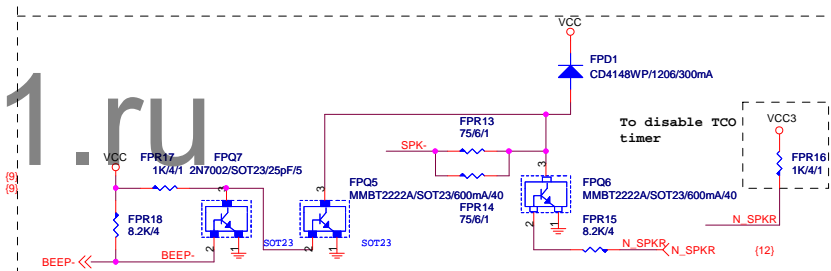
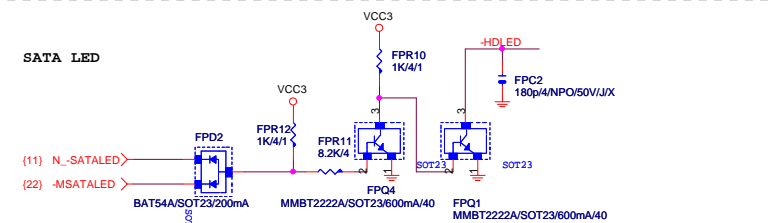
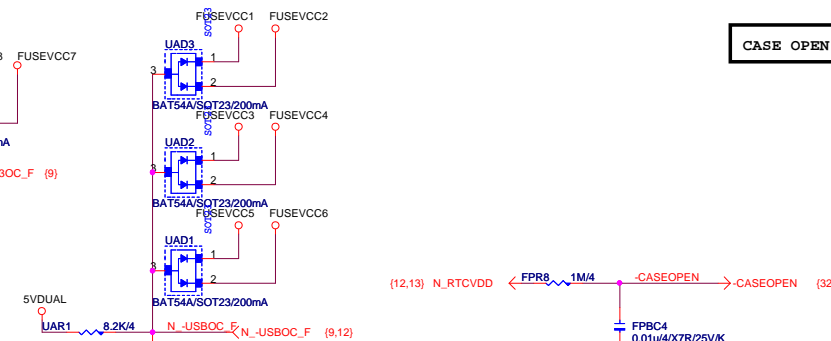
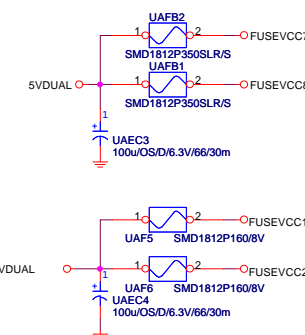


Close to connector

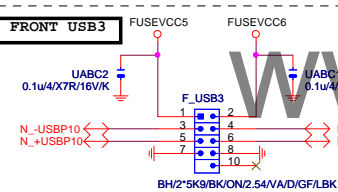


AZ1045-04F/MSOP10

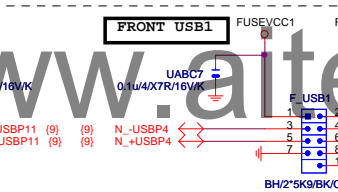
Close to connector



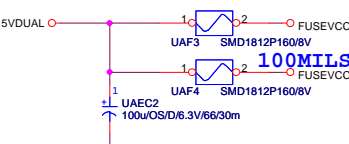
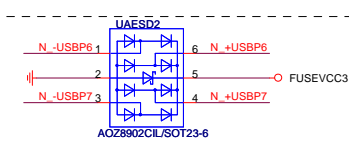
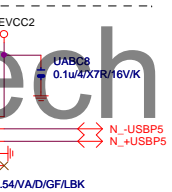
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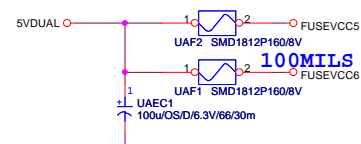
Close to connector



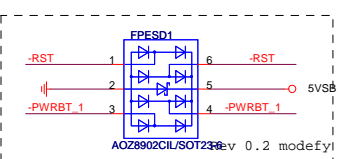
Close to connector



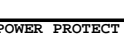
100MILS



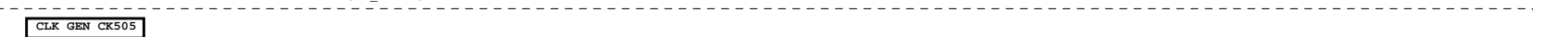
OMILS

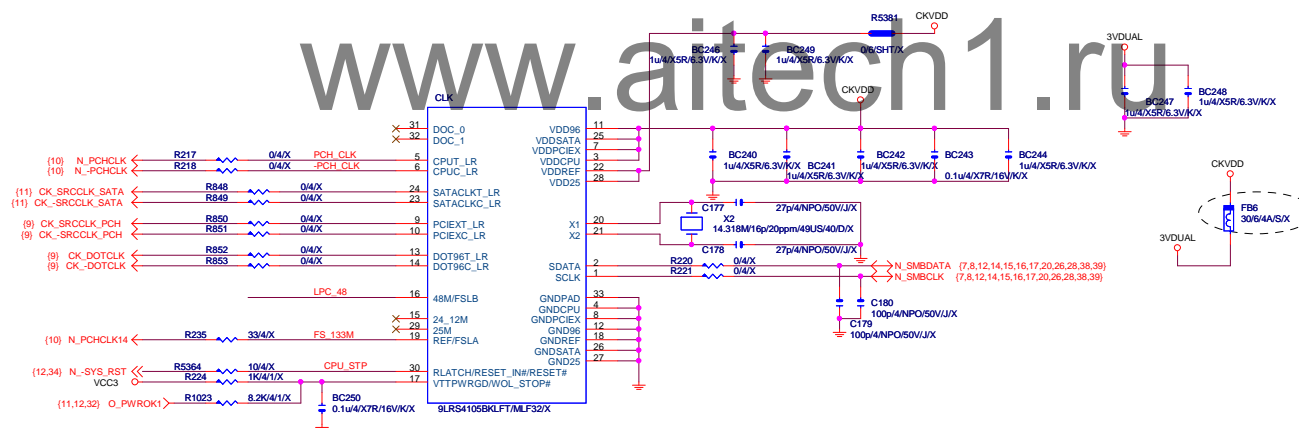
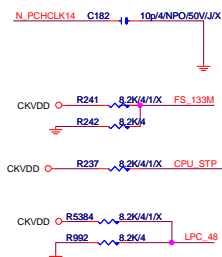


Close to connector



Gigabyte Technology			
Title			
FP,F_USB,BZ			
Size Custom	Document Number	GA-Z77X-UP4 TH	Rev 1.0
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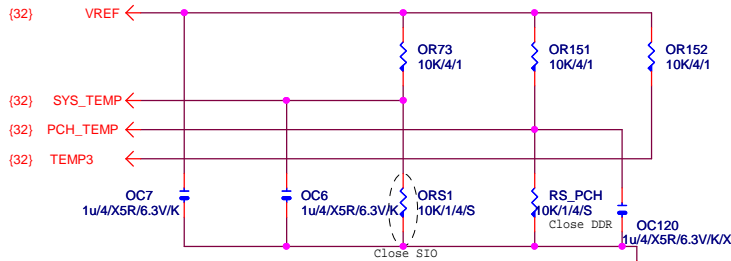




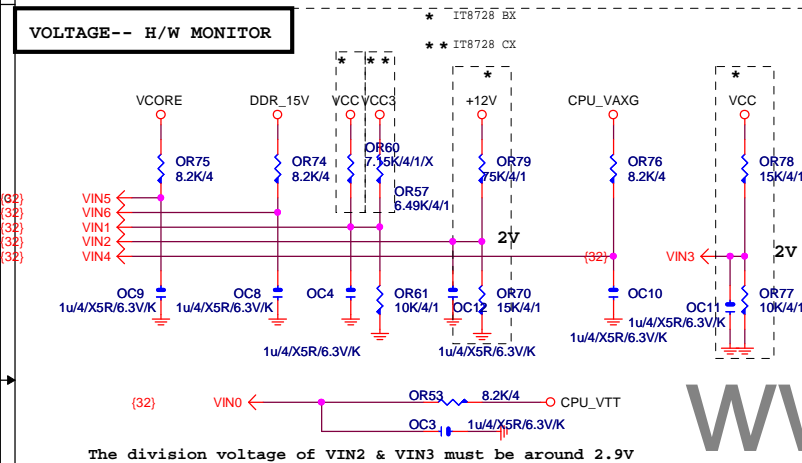
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2	1
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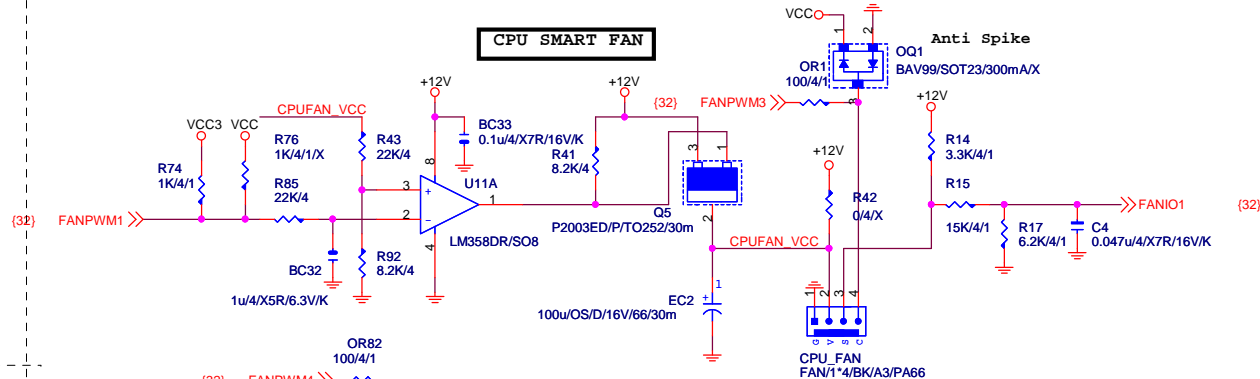
TEMP H/W MONITOR



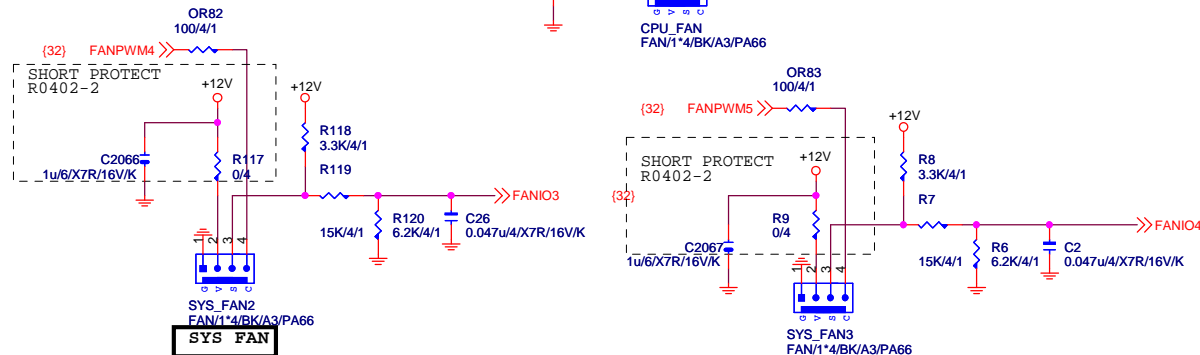
VOLTAGE-- H/W MONITOR



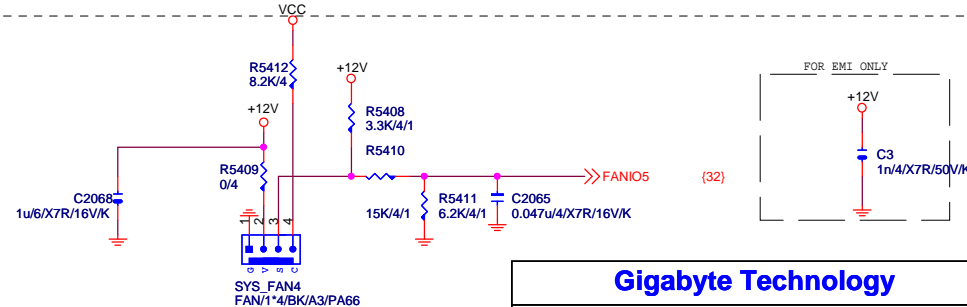
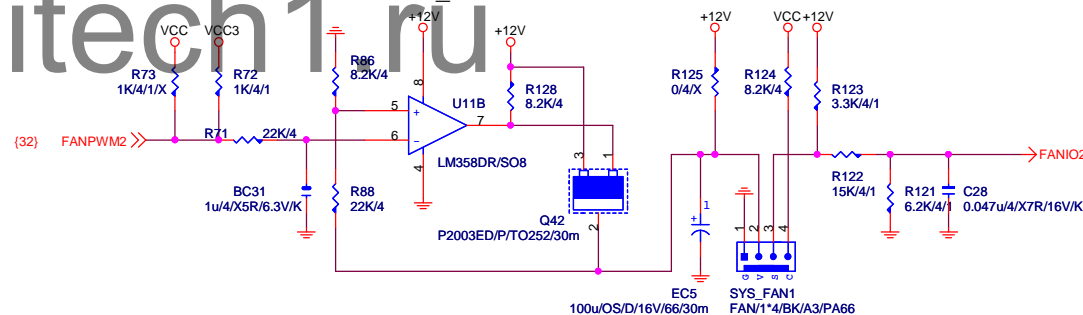
CPU SMART FAN



SYS FAN



Linear SYS_FAN

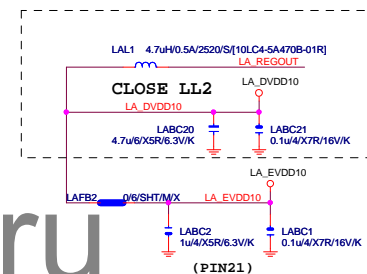
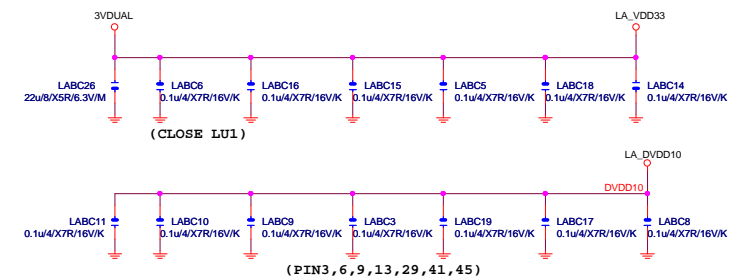
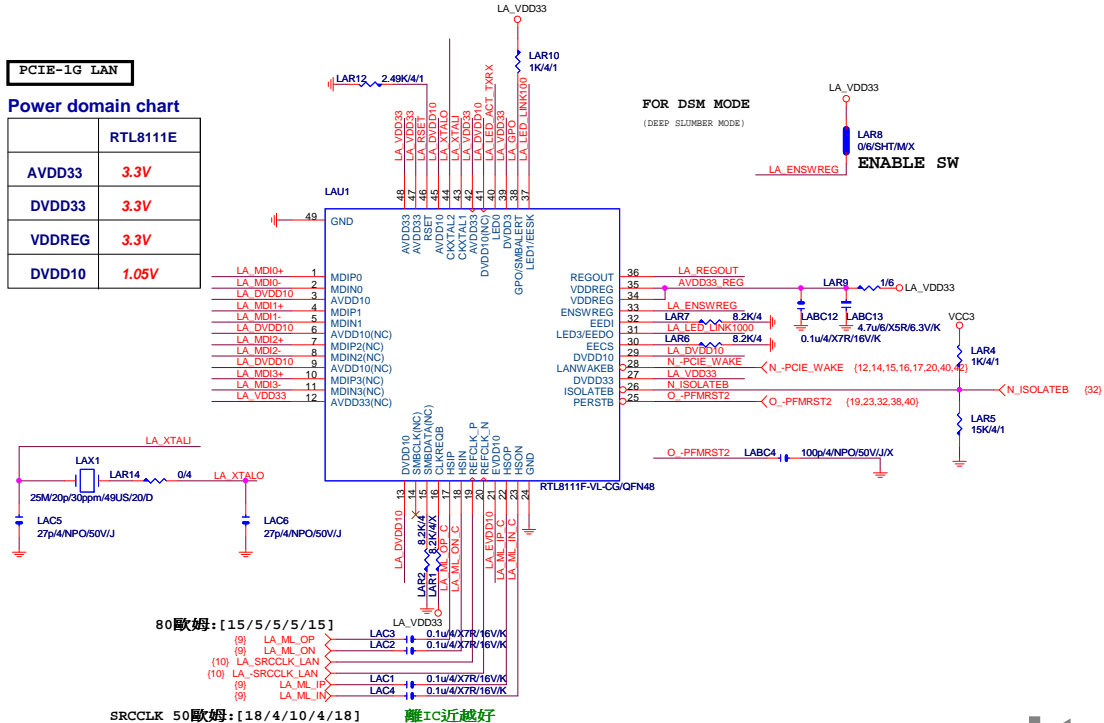


Gigabyte Technology

Title		
HWM,KB/MS, FAN CTRL		
Size	Document Number	Rev
Custom	GA-Z77X-UP4 TH	1.01
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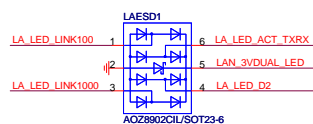
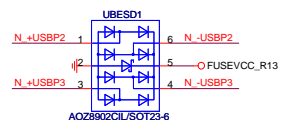
Power domain chart

	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V



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RMA ESD PROTECT



5VDUAL

UEC4

100uF/OS/D/16V/66/30m

C1

C2

LAFB4

SMD1812P350SLR/S

FUSEVCC_R13

LAFB5

SMD1812P350SLR/S

FUSEVCC_R14

1

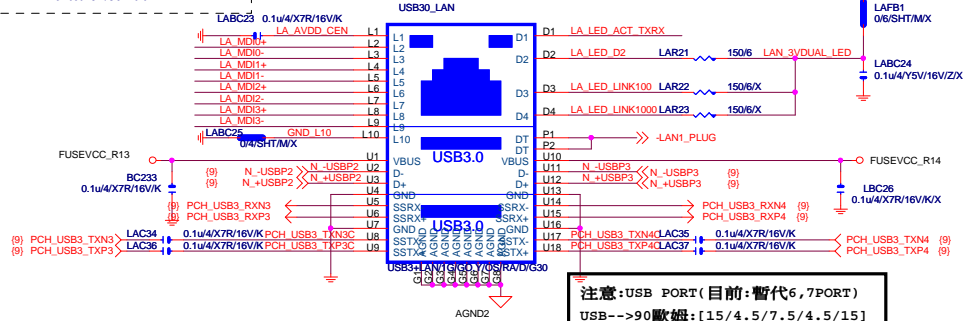
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Close to connector

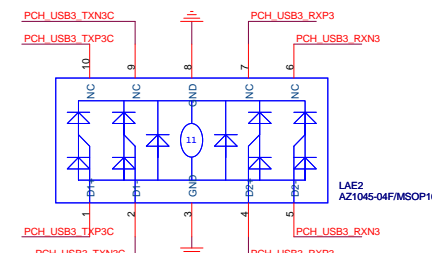
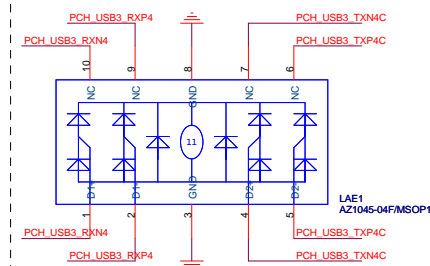
¹ PS:視EMI需求

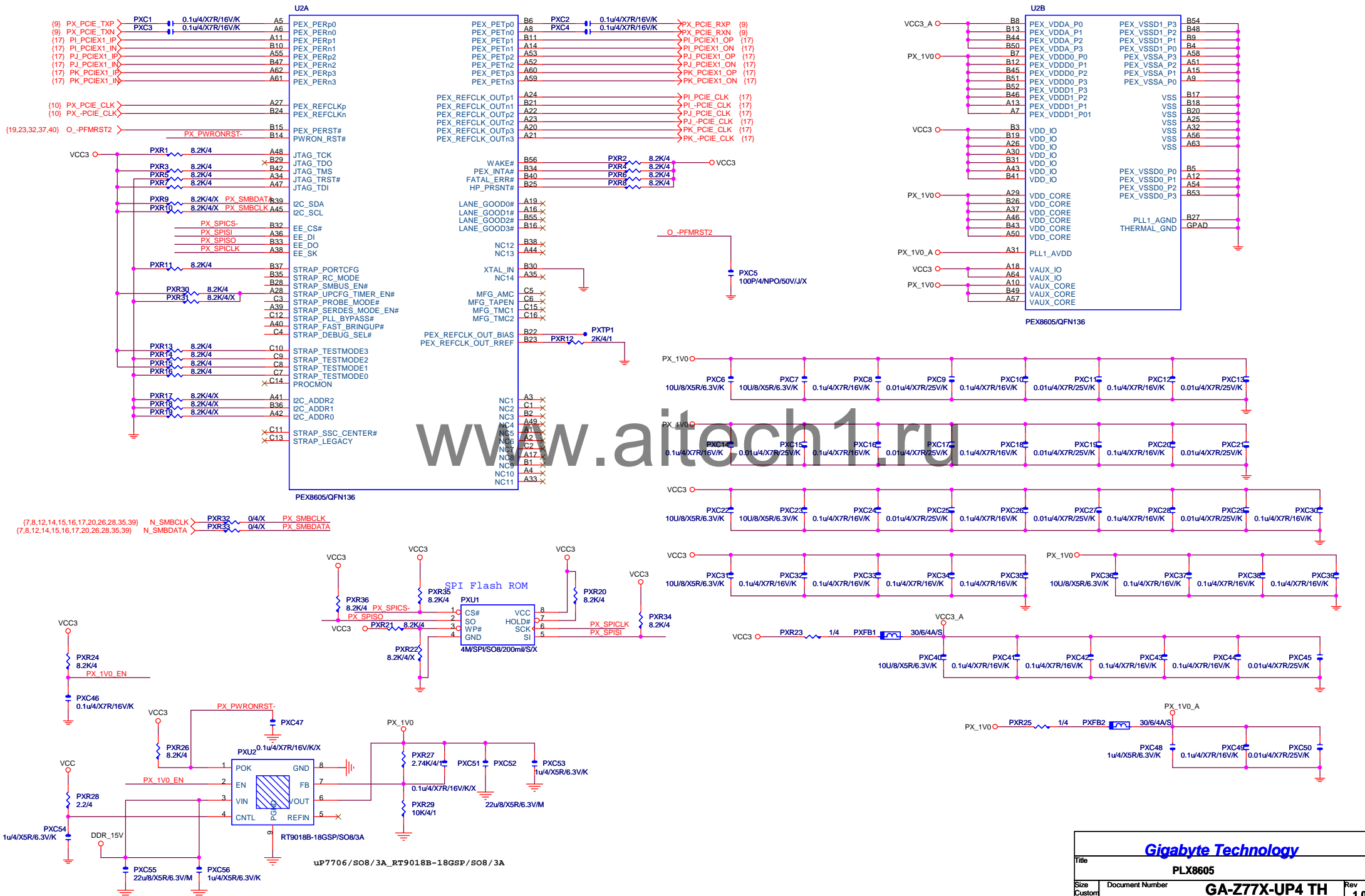


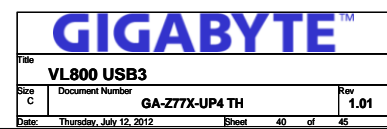
LA MDI-->100歐姆:[20/4/8/4/20]

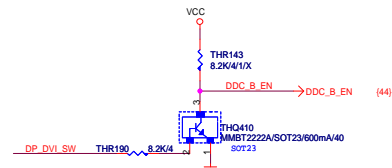
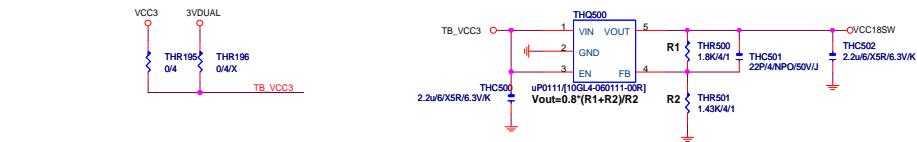
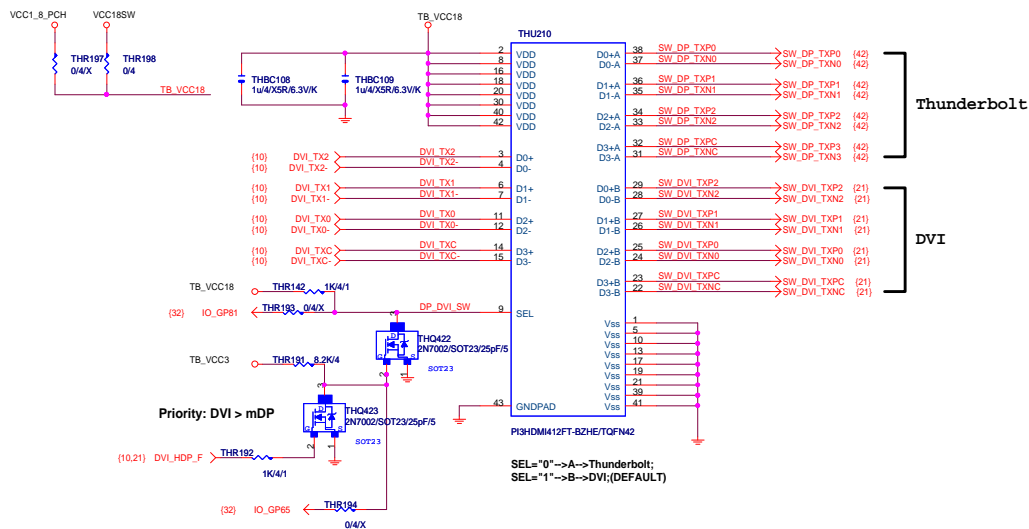


注意:USB PORT(目前:暫代6,7PORT)
USB-->90歐姆:[15/4.5/7.5/4.5/15]



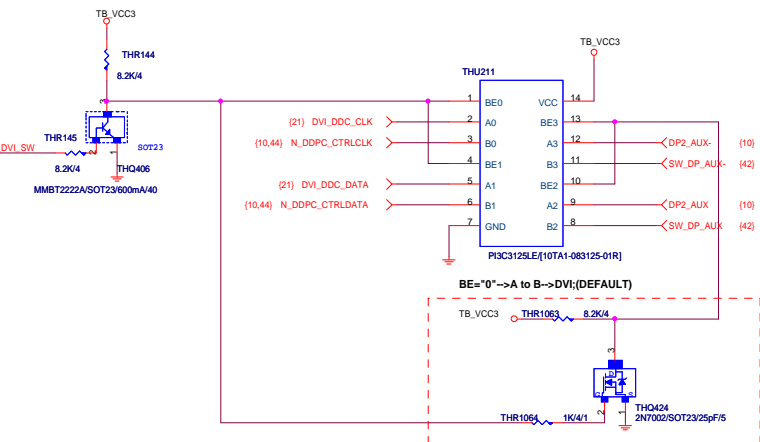




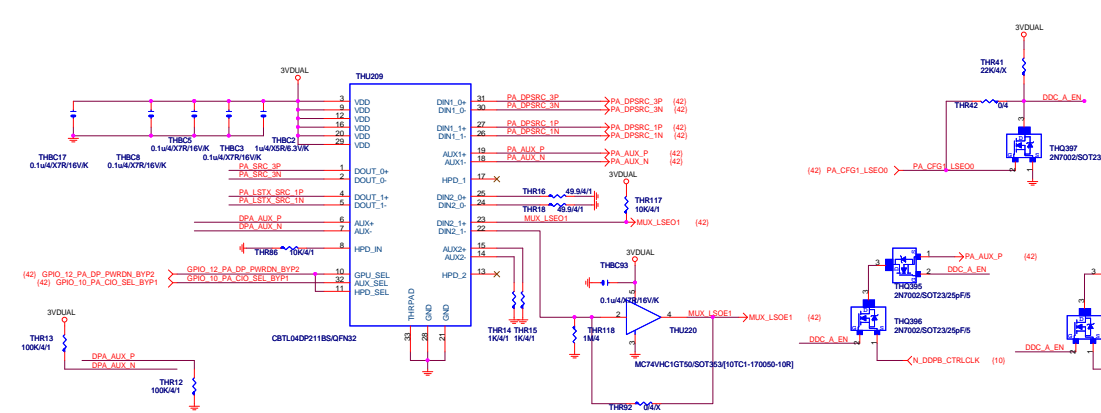


DP_DVI_SW="1"→DDC→PCH to Thunderbolt
DP_DVI_SW="0"→DDC→PCH to DVI(DEFAULT)

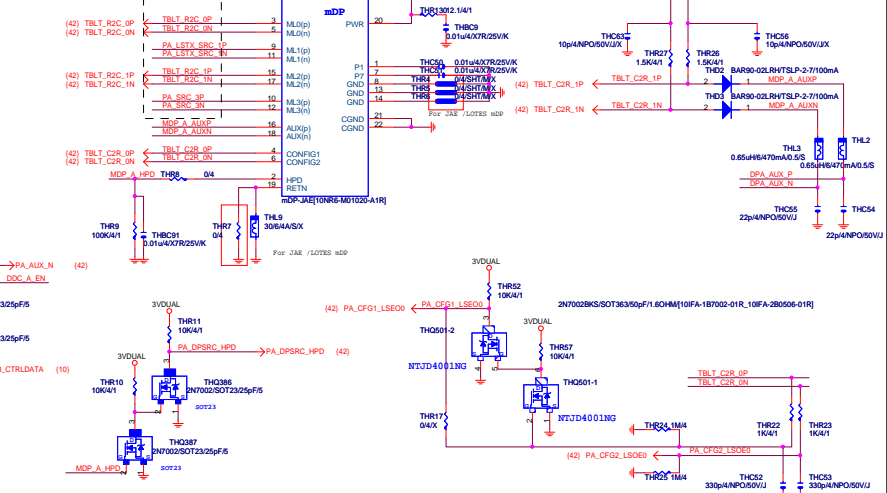
DP_DVI_SW="0"→AUX→PCH to Thunderbolt
DP_DVI_SW="1"→AUX→OPEN



DP_A

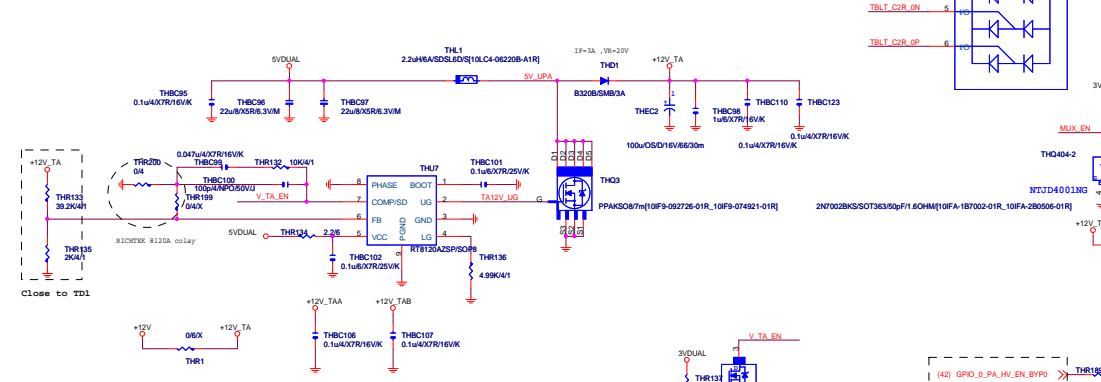


100 speed ,take care layout under 2000mil in whole length

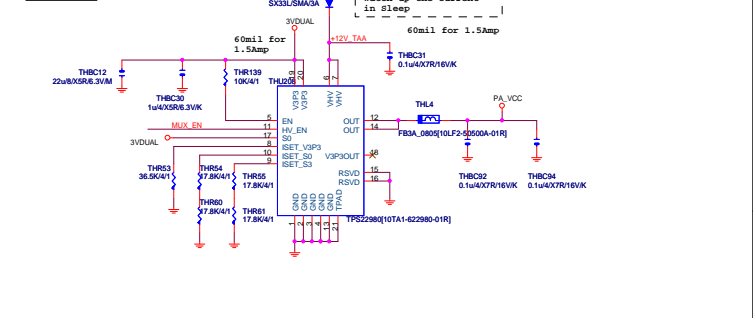


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+12V_TB



MDP_POWER



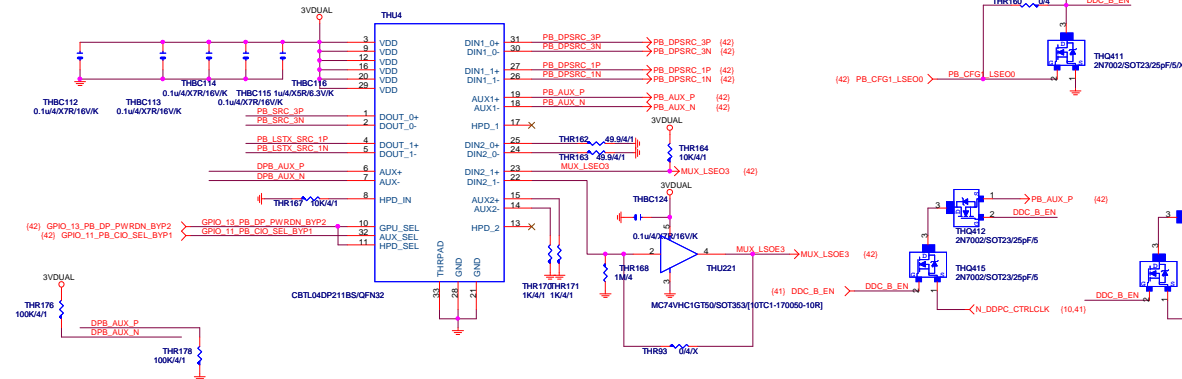
Power Rail	Current budget	S4/S5	S3	S0
VCC3P3_POC	100mA	ON	ON	ON
VCC1_LC	600mA	OFF	ON	ON
VCC1_05_LC	1A	OFF	ON	ON
VCC1_05_CIO	4A	OFF	ON	ON

PA_VCC	Power level	Current budget
S4/S5	3.3V/12V	150mA
S3	3.3V/12V	150mA
S0	3.3V/12V	1.5A

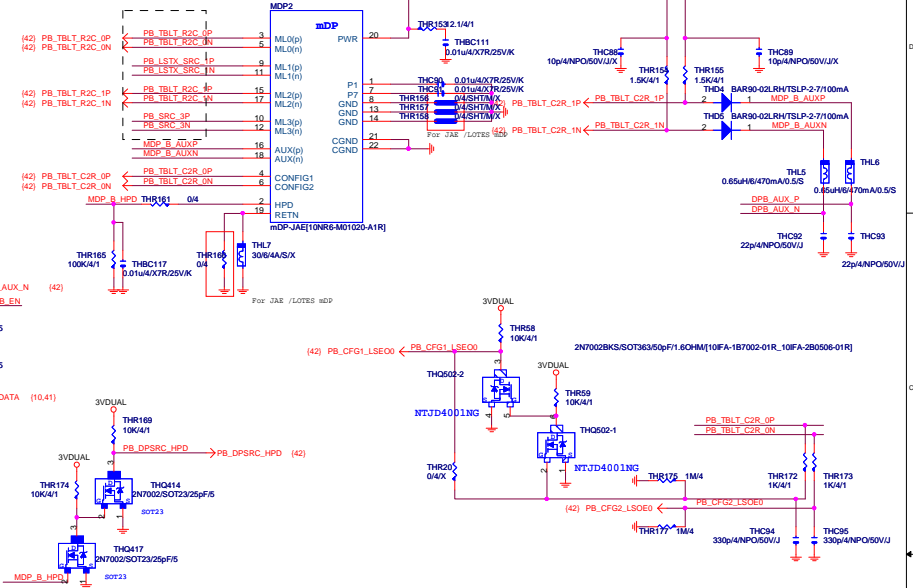
Take care ! S0 mode always active

IN	RV_IN	OUT
0	0	0V
0	1	0V
1	0	V3P3
1	1	VRV

DP_B

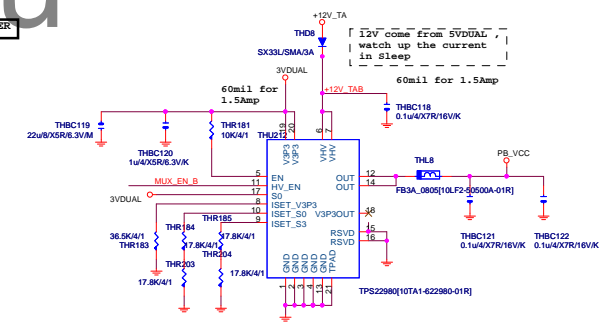
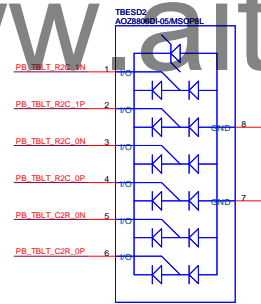


100 speed ,take care layout
under 2000mil in whole
length



Power Sequence
3.3VPOC >> 1.05VLC >> 3.3VLC >> 1.05VCIO

POWER CONSUMTION	
VCC3P3_POC	10mA
VCC3V3_LC	100mA
VCC1V05_LC	2A
VCC1V05_CIO	1.4A



PA_VCC	Power level	Current budget
S4/S5	3.3V/12V	150mA
S3	3.3V/12V	150mA
S0	3.3V/12V	1.5A

Take care ! S0
mode always
active

File	Cactus-Ridge	
Size	Document Number	Rev
	Custom	1.01
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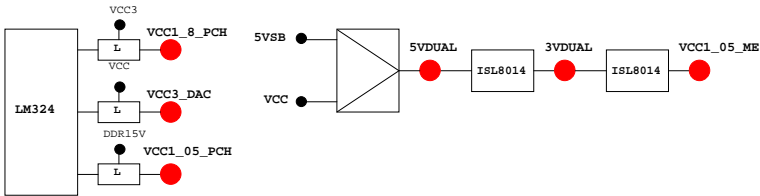
PCH GPIO LIST TABLE

PIN NAME	PWR	Default	USAGE	NOTE
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A
GP1/TACH1	MAIN	GPI	ICH_FAN_TACH1	N/A
GP2/PIRQE#	MAIN	GPI	-PIRQE	P/U 8.2K VCC3
GP3/PIRQF#	MAIN	GPI	-PIRQF	P/U 8.2K VCC3
GP4/PIRQG#	MAIN	GPI	-PIRQG	P/U 8.2K VCC3
GP5/PIRQH#	MAIN	GPI	-PIRQH	P/U 8.2K VCC3
GP6/TACH2	MAIN	GPI	ICH_FAN_TACH2	N/A
GP7/TACH3	MAIN	GPI	ICH_FAN_TACH3	N/A
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL
GP9/OC5#	STBY	NATIVE	OC5#	N/A
GP10/OC6#	STBY	NATIVE	OC6#	N/A
GP11/SMBALERT#	STBY	NATIVE	-SMBALERT	P/U 8.2K 3VDUAL
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL
GP14/OC7#	STBY	NATIVE	OC7#	N/A
GP15	STBY	L	GPO GPIO15	N/A
GP16	MAIN	GPI	-SKTOCC	P/U 8.2K VCC3
GP17/TACH0	MAIN	GPI	ICH_FAN_TACH0	N/A
GP18	MAIN	NATIVE	MB_ID0	P/D 8.2K GND
GP19	MAIN	GPI	-LAN1_ISO	P/U 8.2K VCC3
GP20	MAIN	NATIVE	LED_CTL	P/U 1K VCC3
GP21	MAIN	GPI	VCC18_PCH_OV2	P/U 8.2K VCC3
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3
GP23	MAIN	NATIVE	-LDRQ1	P/U 8.2K VCC3
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL
GP25	STBY	NATIVE	-CPU_STOP	P/U 8.2K 3VDUAL
GP26	STBY	NATIVE	-AC2_DET	P/U 8.2K 3VDUAL
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL
GP29	STBY	L	GPI GPIO29	N/A
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL
GP31	STBY	H-Z	GPI N/A(Reverse)	P/U 8.2K VCC3
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3
GP36	MAIN	GPI	-LAN1_DSM	P/U 8.2K VCC3
GP37	MAIN	GPI	N/A	P/U 8.2K VCC3
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3
GP40	STBY	NATIVE	OC1#	N/A
GP41	STBY	NATIVE	OC2#	N/A
GP42	STBY	NATIVE	OC3#	N/A
GP43	STBY	NATIVE	OC4#	N/A
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL
GP45	STBY	NATIVE	-LPCPME	P/U 8.2K 3VDUAL
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL
GP47	STBY	NATIVE	PSI_LED	P/U 8.2K 3VDUAL
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3
GP50	MAIN	NATIVE	-REQ1	P/U 2.2K VCC
GP51	MAIN	H	NATIVE -GNT1	N/A
GP52	MAIN	NATIVE	-REQ2	P/U 2.2K VCC
GP53	MAIN	H	NATIVE -GNT2	N/A
GP54	MAIN	NATIVE	-REQ3	P/U 2.2K VCC
GP55	MAIN	H	NATIVE -GNT3	N/A
GP56	STBY	NATIVE	N/A(Reverse)	P/U 8.2K 3VDUAL
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL
GP59	STBY	NATIVE	USB_OC0#	N/A
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL
GP61	STBY	L	NATIVE -SUSTAT	N/A
GP62	STBY	L	NATIVE SUSCLK	N/A
GP63	STBY	L	NATIVE GPIO63	N/A
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL
GP73	STBY	NATIVE	1_05V_OV1	P/U 8.2K 3VDUAL
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL

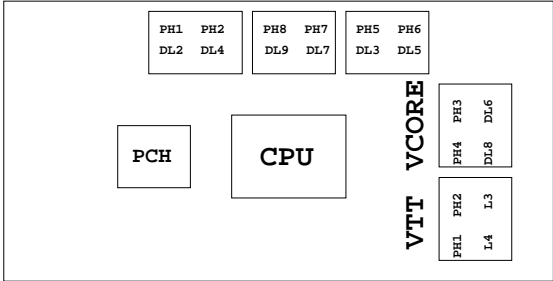
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSS00	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SEC	LOW_PWR_1	
VID05/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSB5W#/GP40	CSI_F0	BSEL166_1
SUSCH#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CsisBSL	
VID00/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AFD#/GP86/SMBC_R	⚡ PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VID01/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT15/CIRRX2/GP16	-THERM	
VID04/GP26/SOUT2	DDR18V_PH2_EN	
VID02/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VID06/GP17/RI2#	1_1V_PH_EN	
VID07/JP6/DTR2#	JP6	
PD5/GP75/BUSS00	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_AVREF_CA_B	DRAM Address Ref
VREF_DQ_AVREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP：
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
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